ARMY
NAVY
AIR FORCE

TM 11-5895-860-34
EE640-CC-MMI-010/E154 RAS
T.O. 31R2-4-474-2

TECHNICAL MANUAL

DIRECT SUPPORT AND GENERAL SUPPORT

MAINTENANCE MANUAL

MAGNETIC DISC, DATA

STORAGE, RANDOM ACCESS

RD-491/TYC-39(V)

(NSN 5805-01-127-0722)

This copy is a reprint which includes current pages from Change 1.

DEPARTMENTS OF THE ARMY, THE NAVY, AND THE AIR FORCE

31 JANUARY 1983

5 SAFETY STEPS TO FOLLOW IF SOMEONE IS THE VICTIM OF ELECTRICAL SHOCK

1. DO NOT TRY TO PULL OR GRAB THE INDIVIDUAL

2. IF POSSIBLE, TURN OFF THE ELECTRICAL POWER

3. IF YOU CANNOT TURN OFF THE ELECTRICAL POWER, PULL, PUSH, OR LIFT THE PERSON TO SAFETY USING A WOODEN POLE OR A ROPE OR SOME OTHER INSULATING MATERIAL

4. SEND FOR HELP AS SOON AS POSSIBLE

5. AFTER THE INJURED PERSON IS FREE OF CONTACT WITH THE SOURCE OF ELECTRICAL SHOCK, MOVE THE PERSON A SHORT DISTANCE AWAY AND IMMEDIATELY START ARTIFICIAL RESUSCITATION

CHANGE

No. 1

DEPARTMENTS OF THE ARMY
THE NAVY, AND THE AIR FORCE
Washington, DC, 17 May 1985

DIRECT SUPPORT AND GENERAL SUPPORT
MAINTENANCE MANUAL
MAGNETIC DISC, DATA STORAGE, RANDOM ACCESS
RD-491 /TYC-39(V)
(NSN 5805-01-127-0722)

TM 11-5895-860-34/EE640-CC-MMI-010/E154 RAS/TO 31R2-4-474-2, 31 January 1983, is changed as follows:

1. Remove old pages and insert new pages as indicated below. New or changed material is indicated by a vertical bar in the margin of the page. Added or revised illustrations are indicated by a vertical bar adjacent to the identification number.

Remove pages	*Insert pages*
A	A and B
2-9 and 2-10	2-9 and 2-10
FO-2 (Sheet 1)	FO-2 (Sheet 1)
FO-2 (Sheet 2)	FO-2 (Sheet 2)
FO-4	FO-4
FO-6	FO-6
FO-7 (Sheet 1)	FO-7 (Sheet 1)
FO-11 (Sheet 1)	FO-11 (Sheet 1)
FO-13 through FO-15	FO-13 through FO-15

2. File this change sheet in the front of the publication for reference purposes.

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WARNINGS

HIGH VOLTAGE

High voltage is used in this equipment. Be careful when working near the interior of the equipment, or near the ac power distribution. Observe warning notes in this technical manual and warning decals on equipment. Death on contact may result if safety precautions are not observed.

USE OF CLEANING SOLVENT

Fumes of TRICHLOROTRIFLUOROETHANE are poisonous. Provide adequate ventilation whenever you use TRICHOLORTRIFLUOROETHANE. DO not use solvent near heat or open flame. TRICHLOROTRIFLUOROETHANE will not burn, but heat changes the gas into poisonous, irritating fumes. DO NOT breathe the fumes or vapors. TRICHLOROTRIFLUOROETHANE dissolves natural skin oils. DO NOT get the solvent on your skin. Use gloves, sleeves and an apron which the solvent cannot penetrate. If the solvent is taken internally, see a doctor immediately.

WARNING

Compressed air shall not be used for cleaning purposes except where reduced to less than 29 pounds per square inch (psi) and then only with effective chip guarding and personnel protective equipment. Do not use compressed air to dry parts when TRICHLOROTRIFLUOROETHANE has been used. Compressed air is dangerous and can cause serious bodily harm if protective means or methods are not observed to prevent chip or particle (of whatever size) from being blown into the eyes or unbroken skin of the operator or other personnel.

INSERT LATEST CHANGED PAGES. DESTROY SUPERSEDED PAGES.

LIST OF EFECTIVE PAGES

NOTE: The portion of text affected by the a vertical line in the outer margins of the page. Changes to illustrations are indicated by miniature pointing hands. Changes to wiring diagrams are indicated by shaded areas.

Dates of issue for original and changed pages are:

Original...0...31 Jan 83
Change...1...17 May 85

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ARMY TM 11-5895-860-34
NAVY EE640-CC-MMI-010/E154 RAS
AIR FORCE T.O. 31R2-4-474-2

TECHNICAL MANUAL
NO. 11-5895-860-34
TECHNICAL MANUAL
EE640-CC-MMI-016/E154 RAS
TECHNICAL ORDER
T.O. 31R2-4-474-2

DEPARTMENTS OF THE ARMY
THE NAVY, AND
THE AIR FORCE

WASHINGTON, DC *31 January 1983*

DIRECT SUPPORT AND GENERAL SUPPORT

MAINTENANCE MANUAL

MAGNETIC DISC, DATA STORAGE, RANDOM ACCESS

RD-491/TYC-39(V)

(NSN 5805-01-127-0722)

REPORTING ERRORS AND RECOMMENDING IMPROVEMENTS

You can help improve this manual. If you find any mistakes or if you know of a way to improve the procedures, please let us know. Mail your letter, DA Form 2028 (Recommended Changes to Publications and Blank Forms), or DA Form 2028-2 located in back of this manual direct to: Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN: DRSEL-ME-MP, Fort Monmouth, NJ 07703.

For Air Force, submit AFTO Form 22 (Technical Order System Publication Improvement Report and Reply) in accordance with paragraph 6-5, Section VI, T.O. 00-5-1. Forward direct to prime ALC/MST.

For Navy, mail comments to the Commander, Naval Electronics Systems Command, ATTN: ELEX 8122, Washington, DC 20360.

In either case, a reply will be furnished direct to you.

LIST OF ILLUSTRATIONS

LIST OF TABLES

CHAPTER 1

INTRODUCTION

Section I. GENERAL

1-1. Scope

This manual describes the Magnetic Disc, Data Storage, Random Access RD-491/TYC-39(V) (fig. 1-1), hereafter referred to as the Random Access Storage (RAS). This manual contains information on the functioning of the equipment and the direct and general support maintenance instructions.

References are made to other publications which cover installation and operation used in conjunction with the RAS. A complete listing of applicable publications is provided in Appendix A. Repair parts authorized for direct and general support are listed in the Repair Parts and Special Tools List (RPSTL) TM 11-5895-860-34P.

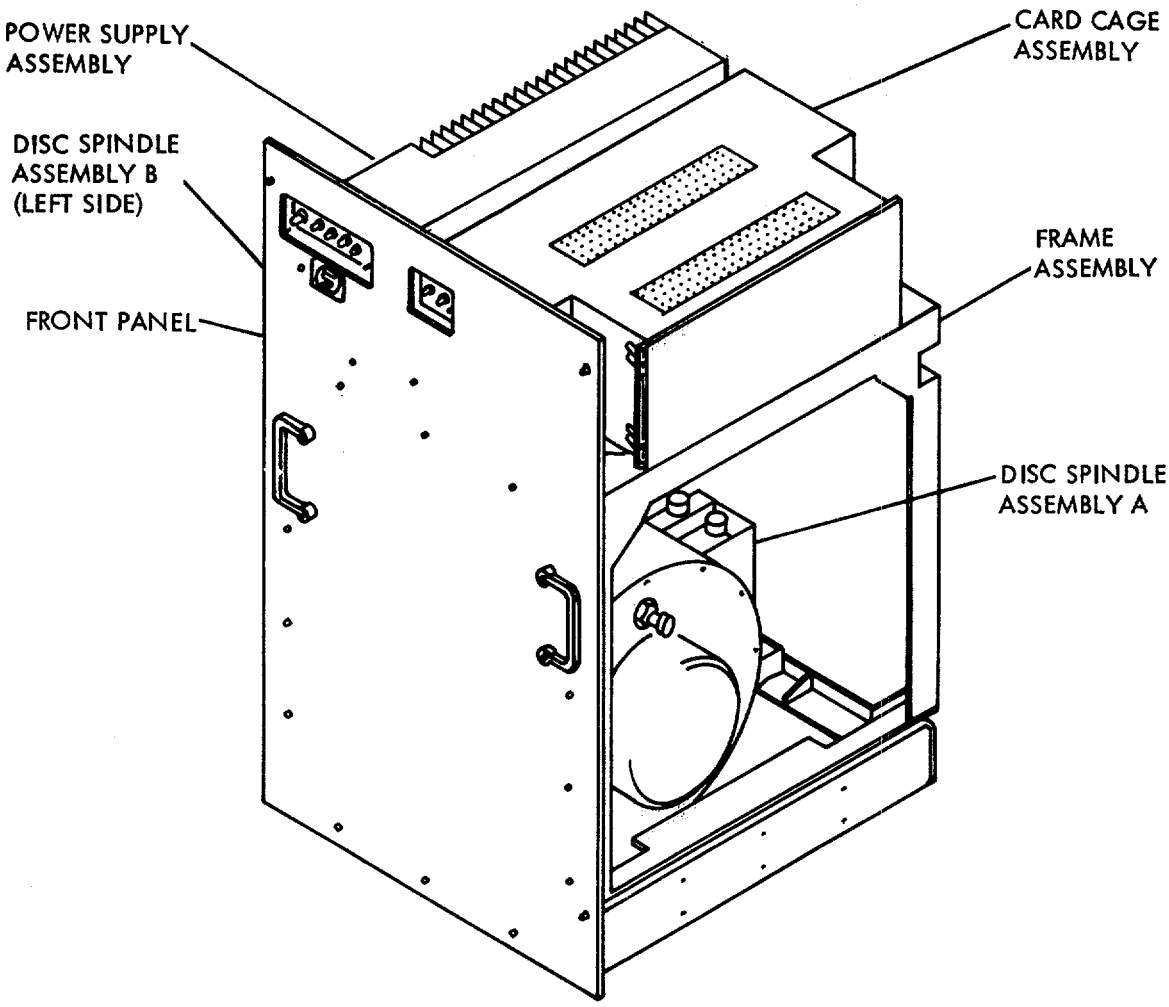


Figure 1-1. Magnetic Disc, Data Storage, Random Access RD-491/TYC-39(V).

1-2. Consolidated Index of Army Publications and Blank Forms.

a. Army. Refer to the latest issue of DA PAM 310-1 to determine whether there are new editions, changes or additional publications pertaining to the equipment.

b. Air Force. Use T.O. 0.1-31 Series Numerical Index and Requirements Table (NIRT).

1-3. Maintenance Forms, Records and Reports

a. Reports of Maintenance and Unsatisfactory Equipment. Department of the Army forms and procedures used for equipment maintenance will be those prescribed by TM 38-750, The Army Maintenance Management System (Army). Air Force personnel will use AFM 66-1 for maintenance reporting and T.O. 00-35D54 for unsatisfactory equipment reporting. Navy personnel will report maintenance performed utilizing the Maintenance Data Collection Subsystem (MDCS) IAW OPNAVINST 4790.2, Vol 3, and unsatisfactory material/conditions (UR submissions) IAW OPNAVINST 4790.2, Vol 2, Chapter 17.

b. Report of Packaging and Handling Deficiencies. Fill out and forward SD 364 (Report of Discrepancy (ROD)) as prescribed in AR 735-11-2/DLAR 4140.55/NAVMATINST 4355.73/AFR 400-54/MCO 4430.3E.

c. Discrepancy in Shipment Report (DISREP) (SF 361). Fill out and forward Discrepancy in Shipment Report (DISREP) (SF 361) as prescribed in AR 55-38/NAVSUPINST 4610.33B/AFR 75-18/MCO P4610.19C/ DLAR 4500.15.

1-4. Reporting Equipment Improvement Recommendations (EIR).

a. Army. If the Magnetic Disc, Data Storage, Random Access RD-491/TYC-39(V) needs improvement, let us know. Send us an EIR. You, the user, are the only one who can tell us what is not liked about your equipment. Let us know why you do not like the design. Put it on an SF 368 (Quality Deficiency Report). Mail it to Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN: DRSEL-ME-MP, Fort Monmouth, NJ 07703. We will send you a reply.

b. Air Force. Air Force personnel are encouraged to submit EIRs in accordance with AFM 900-4.

c. Navy. Navy personnel are encouraged to submit EIRs through their local Beneficial Suggestion Program.

1-5. Administrative Storage

Administrative storage of equipment issued to and used by Army activities will have preventive maintenance performed in accordance with the Preventive Maintenance Checks and Services (PMCS) charts. (Refer to TM 11-5805-681-12 or TM 11-5805-683-12-1 before storing.) When removing the equipment from administrative storage, the PMCS should be performed to assure operational readiness. Disassembly and repacking of equipment for shipment or limited storage are also covered in TM 11-5805-681-12 and TM 11-5805-683-12-1.

1-6. Destruction of Army Electronics Materiel

Destruction of Army electronics materiel to prevent enemy use shall be in accordance with TM 750-244-2.

Section II. DESCRIPTION AND DATA

1-7. Purpose and Use

The RAS operates in conjunction with a controller and accepts serial data and sync bits. The RAS encodes and stores the data on magnetic discs, and retrieves the data on command.

1-8. Description

The RAS is a disc-type magnetic memory unit consisting of two disc spindle assemblies, a power supply, a card nest, and a frame assembly. Refer to TM 11-5805-683-12-1 for a general description and illustrations of the equipment, operating instructions, and organizational maintenance instructions.

1-9. Tabulated Data

Refer to TM 11-5805-683-12-1 for tabulated listings of technical characteristics.

CHAPTER 2

FUNCTIONING OF EQUIPMENT

Section I. FUNCTIONAL DESCRIPTION

2-1. Scope

The RAS operates in conjunction with the random access storage controller (RASC) and accepts input bit-serial and sync data, and encodes and stores the data as magnetic dipoles at a specified location on the disc surface. Data content and storage address are determined by the data processing control unit. When commanded to retrieve information from a specific address, the RAS locates the data, transforms the recorded flux patterns to an encoded analog signal, and decodes the readback waveform to a nonreturn to zero (NRZ) format. All data transfers are timed by the disc system clocks.

2-2. Functional Description

Input/output logic consists of interface drive and receive circuits which are the communication link between the RAS and RASC. The input/output control logic responds to commands from the RASC and provides logic interface and status to the RASC. The read/write electronics consists of data storage timing and read/write electronics required to write data on and read data from the magnetic disc. The magnetic disc houses the storage medium, read/write head assemblies, and disc spindle drive motor. The power supply provides all the necessary dc voltages for the RAS operation.
Figure 2-1 is a functional block diagram of the RAS.

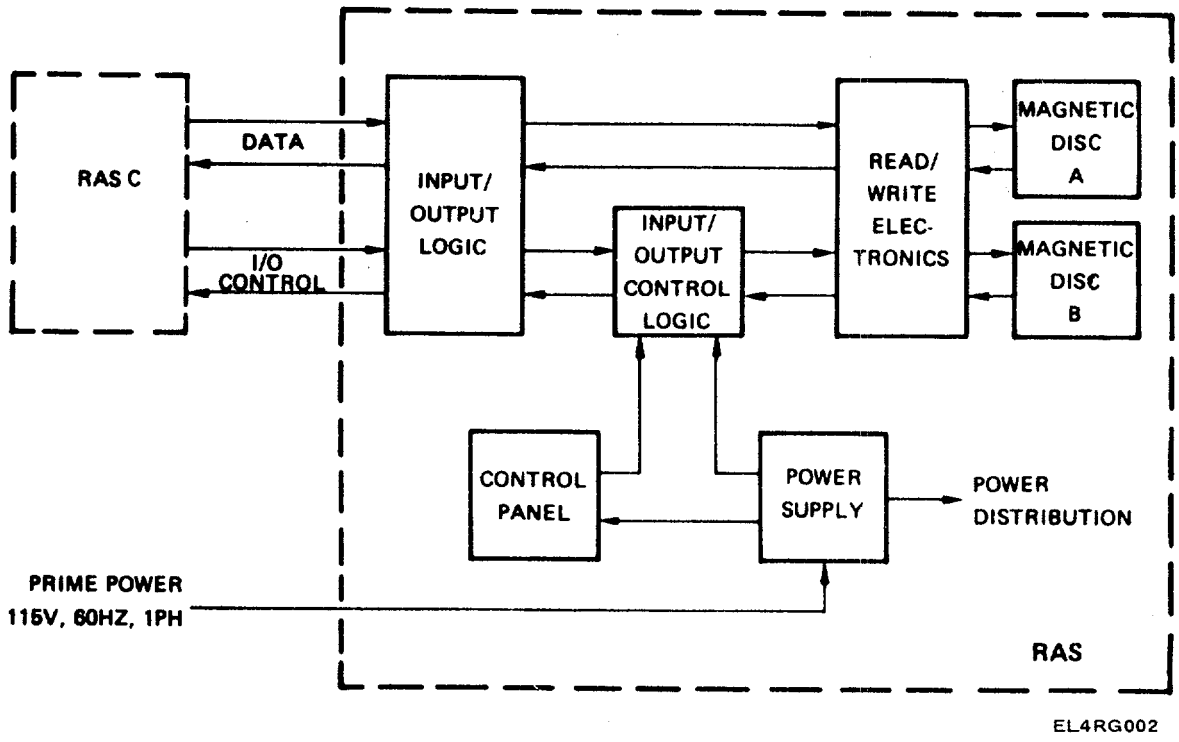


Figure 2-1. RAS Functional Block Diagram

2-3. RASC/RAS Interface

The RASC and RAS interfaces are shown in figure 2-2. The input/output logic levels: Logical 1 = 0.25 ± 0.25v (true); Logical 0 = 3.95 ± 1.55v (false). The functions of each interface are as follows:

a. RAS SELECT. The high active signal on one-of-two select lines will activate the RAS with the corresponding unit number and enable it to receive all subsequent signals from the controller. The RAS select signal must remain high active for the duration of the operation. A low level signal will terminate any disc operation.

b. TRACK ADDRESS. The ten-track address lines provide the selected RAS with track address signals in binary form. A low active signal indicates a logic 1.

c. WRITE DATA. Upon receipt of a write enable command, write data is transferred synchronously with the read/write clock. A low active signal specifies a logic 1 is to be written.

d. WRITE ENABLE. A low active signal will enable the write circuits of the selected RAS.

e. READ ENABLE. A low active signal will enable the read circuits of the selected RAS.

f. ERROR RESET. A low active signal will reset the Clock Error and Parity Error of the selected RAS.

g. READY DISK. Only one-of-four ready lines will be low active when the RAS is able to perform a read or write operation.

h. SECTOR ADDRESS. The selected RAS transmits the disc's Sector Address in binary form to the RASC on the seven sector address lines. A low level signal indicates a logic 1.

i. SECTORS ADDRESS STROBE. A low active signal indicates that the sector address lines of the selected RAS are energized and stable.

j. SECTOR CLOCK. At the beginning of each sector, a low active signal is sent from the selected RAS to the RASC.

k. MASTER CLOCK. The master clock signal is transferred from the selected RAS to the RASC on this line.

l. INDEX CLOCK. A low active signal on this line indicates the start of a new disc revolution.

m. READ/WRITE CLOCK. When data is being transferred during a read or write operation, the Read/Write Clock signal is sent from the selected RAS to the RASC on this line.

n. READ DATA. Upon receipt of a read enable command, read data is transferred from the selected RAS synchronously with the read/write clock. A low active signal indicates a logic 1 has been read.

o. CLOCK ERROR. Upon detection of Clock Error, the selected RAS will terminate operation and transmit a low active signal to the RASC. This line will remain low until the Error Reset signal is received from the RASC.

p. PARITY ERROR. Upon detection of Parity Error (even parity) the selected RAS will transmit a low active signal to the RASC. This line will remain low until the Error Reset signal is received from the RASC.

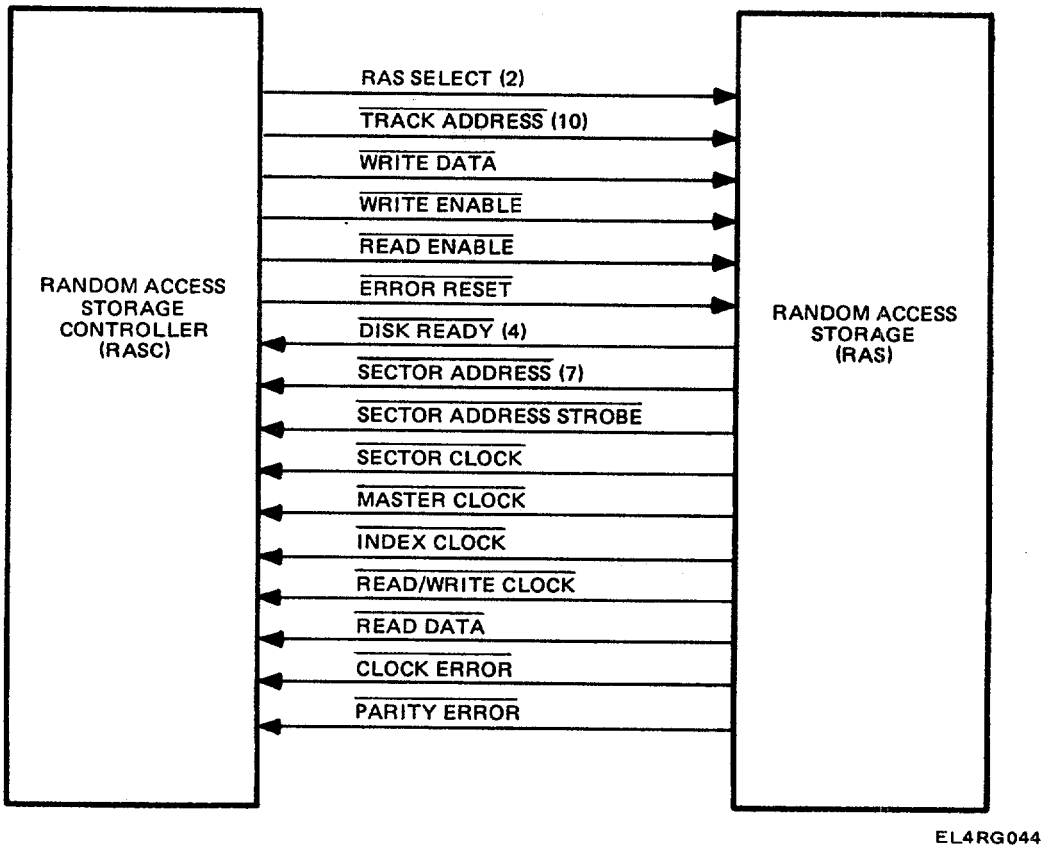


Figure 2-2. RASC/RAS Interface Block Diagram.

2-4. Track Address Line Coding

The ten track address lines **TRK ADD 0** through **TRK ADD 9)** from the RASC (fig. 2-3) are used to select one of 1024 read/write heads available in the RAS. The track address lines are identified by digits 0 through 9 in numerical order. Each track address line represents one numerical position in the ten-place binary number, with TAO representing the least significant bit position. TAO through TA4 are decoded to select the corresponding one of thirty-two center taps (selection drivers). TA5 through TA7 are decoded to select the corresponding one of eight trunks. TA9 is decoded to select spindle A or B containing the selected read/write head. TA8 is decoded to select disc sides one of two of the selected disc spindle assembly. The track address lines from the RASC are received and inverted before being distributed throughout the RAS system by the Interface Logic.

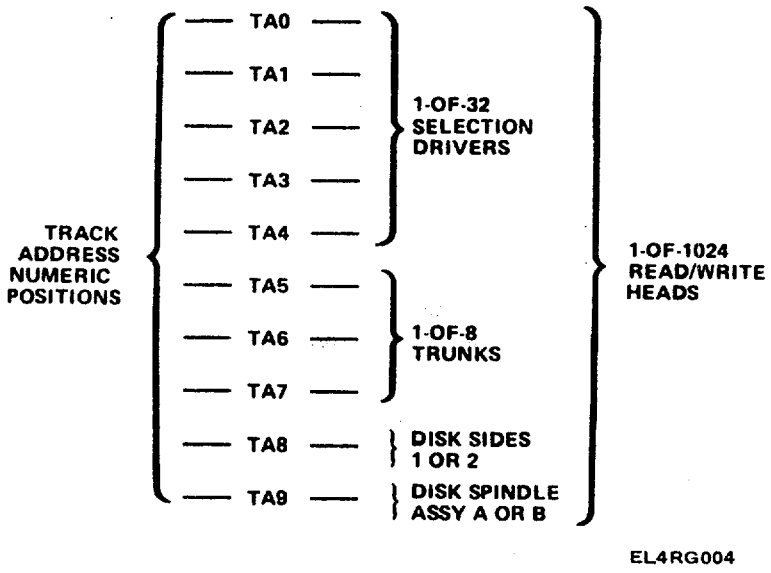


Figure 2-3. Track Address Line Decoding Diagram.

a. *TA9*. TA9, when low, enables disc spindle assembly A and its associated circuit cards. When TA9 is high, disc spindle assembly B and its associated circuit cards are enabled. TA9 is sent to Control Logic to select either drive A or B Clock Amplifier output signals. TA9 is also used to generate **DISK SEL** (A or B) (FO-2). DISK SEL is sent to the Clock Amplifier to gate **SECTOR ADDRESS LINE** (0 through 6) to the controller.

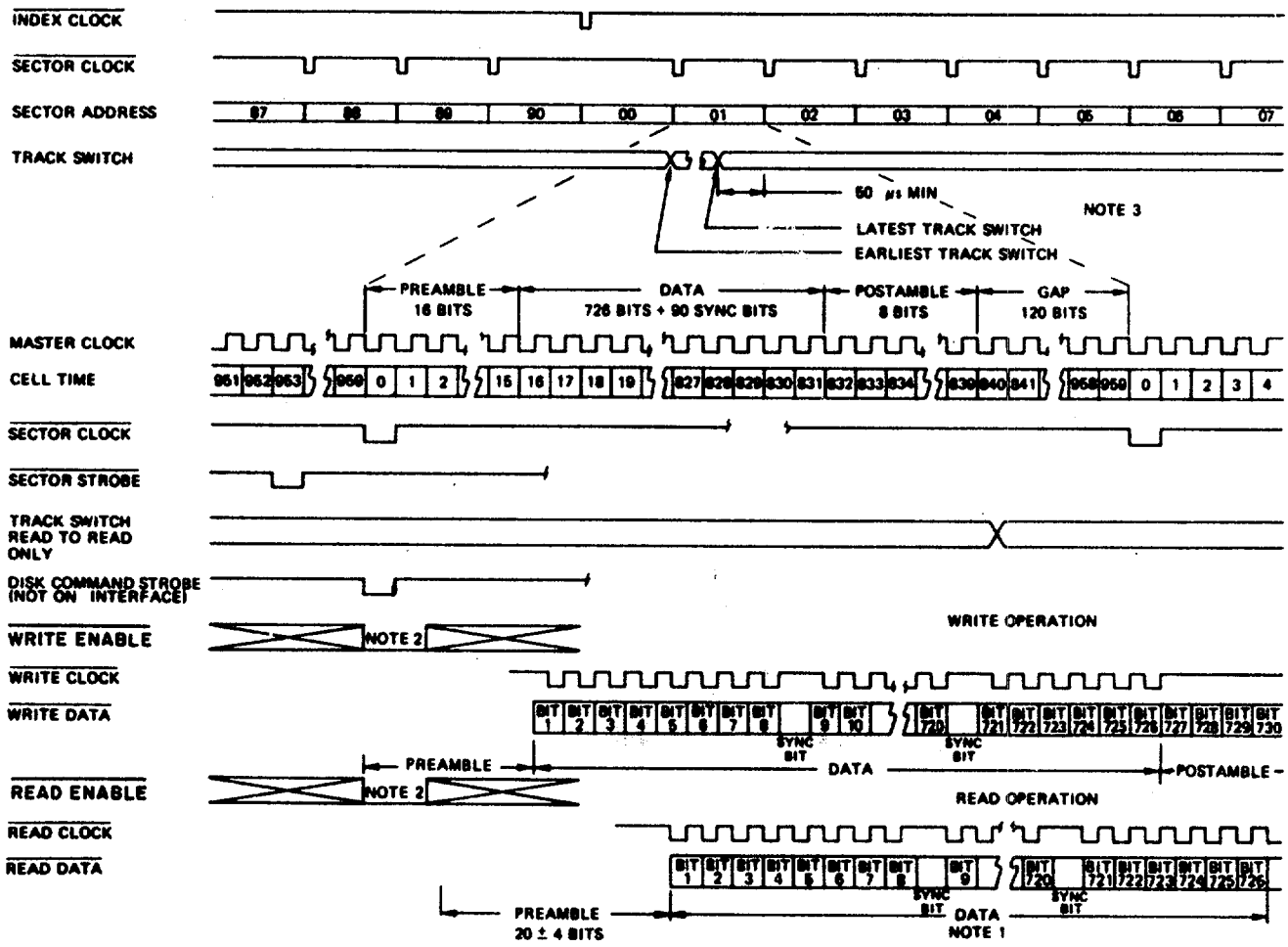
b. TA0 through TA4. TA0 through TA4 is sent to the Selection Driver and Spare Track Select Logic. In the Selection Driver, TA0 through TA4 are decoded to select one of thirty-two center taps which is sent to both disc spindle assemblies A and B. In the Spare Track Select Logic, TA0 through TA4 are combined with TA5 through TA8 and tested for sparing.

c. TA5 through TA8. TA5 through TA8 are sent to the Spare Track Select Logic to be combined with TA0 through TA4 and tested for sparing. The outputs TA5 and TA6 are sent to their respective (four of eight) Quad Write/Preamplifiers. Outputs TA7 and TA8 are sent back to the Interface Logic where they are decoded to generate one of four **TRUNK SEL** (0 through 3). **TRUNK SEL** enables its corresponding Quad Write/Preamplifier, allowing TA5 and TA6 to be decoded, thereby selecting one of four trunk lines. The selected trunk line and center tap are sent to a 16 X 32 matrix to select a specific read/write head core in the disc spindle assembly.

d. Spare Track. When a spare track is selected (hard-wired in Spare Track Select Logic), new values for TA5 through TA8 are generated and sent to their corresponding Quad Write/Preamplifiers and Interface Logic. The center tap disable **CT DISABLE** is applied and sent to the Selection Driver to disable the unusable head core. A spare center tap SCT (0A, 1A, 0B, or 1B) signal is applied. The selected trunk line and SCT are sent to a 16 X 32 matrix to select a specific spare read/write head core in the disc spindle assembly.

2-5. Track Format

A single track is divided into 91 sectors (fig. 2-4). Each sector is 960 bits long, and begins with a 16-bit preamble, consisting of 15 ONEs followed by a ZERO. This preamble time is used by the system to begin read amplifier operation and to synchronize the read clock with the data. The data (8'6 bits) consists of 726 data bits plus 90 sync bits. A sync bit is written after every eighth data bit. At the end of data, an 8-bit postamble (consisting of seven ONEs followed by a ZERO) is written, followed by a 120-bit sector gap. The postamble protects the last data bit from end-point deterioration, and the gap provides time for switching tracks. The sync bit generated by the RAS is a logic ONE inserted in the serial NRZ data stream. The write electronics causes a flux reversal at the end of the cell time for each ONE of the data (including the sync bits). No flux reversals are written for ZEROs. The sync bit provides a periodic reversal in a long string of ZEROs to enable synchronization of a phase-locked loop read clock circuit.



NOTES:

1. DUE TO LOGIC DELAYS AND THERMAL SKEW ALLOWANCES, READ DATA IS DELAYED 4 ± 4 BITS FROM CORRESPONDING BIT OF WRITE DATA.
2. READ AND WRITE ENABLE LINE TO BE STABLE FOR TWO CELL TIMES MINIMUM, FOLLOWING LEADING EDGE OF CELL TIME 0.
3. TRACK SWITCH BETWEEN SECTOR MARK AND 50 µs PRIOR TO FOLLOWING SECTOR.

EL4RG003

Figure2-4. RAS Timing Diagram

2-6. Data Storage

The data pattern is stored as a series of magnetic dipoles. Each read/write head contains multiple coils with both leads of each coil connected to a trunk line through diodes. Only one coil is active at a time and the inactive coils are reverse biased with -12v through a center tap. During a write operation, a forward bias to the center tap of a selected coil enables the coil, and write current is then directed alternately through one half and then the other half of the coil by the write amplifier. The direction of current flow determines polarity of the recorded dipole. During a read operation, as the disc surface rotates past the enabled head coil, the magnetic flux path of each dipole is cut by the coil and a voltage is induced across the full winding. The dipole polarity determines the direction of the read-back waveform. The recovered signal is decoded, synchronized with read clock, and presented to the interface.

2-7. Write Operation

The **WRITE ENABLE** and **WRITE DATA** (fig. FO-2) from the RASC are input to the Control Logic. **WRITE ENABLE** is strobed and stored at the trailing edge of **SECTOR CLOCK**. **WEN-1, WEN-2** and **WCLK-1** through WCLK-4 are generated and distributed to eight Quad Write/Preamplifier circuit cards. The appropriate circuit card is enabled by one of eight **TRUNK SEL** lines. Track address lines TA5 and TA6 are decoded to select one of four trunk lines. The **AGC RESET** is applied coincident with **WEN-1** and **WEN-2,** and sent to the Data Read Amplifier to minimize the gain of the input amplifier. Write enable WEN-1, WEN-2, and EN SEL end 2-1/2 bits before SECTOR ADDRESS STROBE for the next sector. AGC RESET remains applied until WC53 and EN SEL is applied at WC53 of the next sector if the next sector is not a Write Operation. Sequence of WCLK-x (encoded write data) is as follows:

a. 16 bits of preamble.

b. Eight bits of controlled data.

c. One sync bit (a " 1").

d. Sequence b. and c. repeated until 726 bits of controlled data are recorded.

e. The remainder of the sector is written with eight bits of postamble and 120 bit of gap.

2-8. Read Operation

READ ENABLE (fig. FO-2) from the RASC is strobed and stored by the Control Logic at the trailing edge of **SECTOR CLOCK**. The read sequence is as follows:

a. Read enable **REN** to the Data Read Amplifier is applied seven bits after **SECTOR CLOCK**.

b. Nine bits after **REN**, the RD stream from the Data Read Amplifier is monitored for the final zero of the preamble code.

c. The **READ DATA** and **READ/WRITE CLOCK** are sent to the RASC.

d. After every eighth bit, the clock bit is stripped from **READ/WRITE CLOCK**.

e. After the 726th **READ DATA**, the bit is sent to the controller, **READ/WRITE CLOCK** is stopped, **REN** is reset and the sector read is completed.

Section II. CIRCUIT DESCRIPTION

2-9. Interface Logic

The Interface Logic (fig. FO-3) decodes track address signals from the RASC for unit/track selection. When the RASC applies RAS SEL 1, the RAS with its UNIT SEL switch in the 1 position will respond and vice versa. If the input to gate U7A is high, **UNIT 1** is applied. With **UNIT 1** and **RAS SEL 1** low, and **RAS SEL 2** and **UNIT 2** high, **RAS SEL** is generated and sent to both Spare Track Select Logic A and B, and to the Control Logic. When **RAS SEL** is high, the RAS will not respond to the RASC. Both **DISK A OK** and **DISK B OK** from the Control Logic are applied. **UNIT 1** enables the logic circuit and developes **RDY DISK 1A** and **RDY DISK 1B**, which are sent to the RASC. **TRK ADD 0** through **TRK ADD 9** from the RASC are inverted in the Interface Logic. TAO through TA8 are sent to both Spare Track Select Logic A and B. TA0 through TA4 are also sent to the Selection Driver. Spare Track Select Logic circuit card A is selected when TA9 is high and circuit card B is selected when TA9 is low. With TA9 and EN SEL both low, TA7A and TA8A will assert one of four **TRUNK SEL** (OA through 3A). The applied **TRUNK SEL** is sent to one of four Quad Write/Preamplifier circuit cards in spindle A. With TA9 and **EN SEL** both low, TA7B and TA8B will assert one of four **TRUNK SEL** (OB through 3B). The applied **TRUNK SELECT** is sent to one of four Quad Write/Preamplifier circuit cards in spindle B.

2-10. Selection Driver

The Selection Driver (fig. FO-4) drives the center taps of the read/write heads. This circuit card consists of 32 selection drivers. Each selection driver is connected to both Spindle Housing Assemblies A and B (hereafter

referred to as Disc Spindle Assembly) and isolated from one another by diodes CR2 and CR3 on the circuit card. To select one of 32 selection drivers (SDO-SD31), **CT DISABLE A** and **CT DISABLE B** must remain high. The decoded TA3 and TA4 outputs select one of four track address decoders (U3 through U6). The decoded TAO, TA1, and TA2 outputs select one of eight selection drivers of the selected decoder.

2-11. Spare Track Select Logic

There are two identical Spare Track Select Logic circuit cards (A and B) in the Card Cage Assembly. Circuit cards A and B are connected to Disc Spindle Assemblies A and B, respectively. The Spare Track Select Logic (fig. FO-5) allows the maintenance technician to substitute a spare head/track circuit in place of a head/track circuit that has failed. The Spare Track Select Logic is enabled by TA9 and **RAS SEL**, both being low. TA4 low enables decoder UI and inhibits decoder U2. TA4 high enables U2 and inhibits U1. When a head/track circuit is spared, the selected one of 32 gate outputs (SO through S31) enables one of four encoders (U4 through U7). The output of the selected encoder is decoded and the new values for TA5 through TA8 are developed and applied to multiplexer U8. The new values for TA5 and TA6 are sent to the Quad Write/Preamplifiers. The new values for TA7 and TA8 are sent to the Interface Logic. The GS output of the selected encoder will always be low; therefore, the output of gate U 18B is gated high. This causes **CT DISABLE** to be asserted and disables the Selection Driver. The high output of gate U18B also allows U8 to pass all TAX inputs. The low GS output of encoders U4 and U6 selects spare center tap SCTO. The low GS output of encoders U5 and U7 selects spare center tap SCT1. The spare center taps SCTO and SCT1 are connected to the Matrix Interconnect circuit boards in the Disc Spindle Assembly.

2-12. Matrix Interconnect

The RAS contains two identical Disc Spindle Assemblies operating independently of each other. Both disc spindle assemblies contain two identical Matrix Interconnects and provide 1024 active tracks plus 64 spare tracks for manufacturing and corrective maintenance purposes. Each side of both disc spindle assemblies 8 X 32 matrix of 256 tracks. The RASC selects a track for recording or retrieving data. The selected track is activated by means of a 32 X 32 matrix. One of the two matrix coordinates is comprised of 32 sets of "trunks" from 32 sets of write amplifiers and preamplifiers. The other matrix coordinate is comprised of 32 "selection drivers". The read/write heads are woven into a matrix interconnect (fig. FO-6) in the following manner. Each head coil is center-tapped, and the coil ends are isolated by diodes. The coil center-taps are connected together in 32 groups of eight, each group connected to one selection driver and forming one row of the matrix coordinates. The diodes at each end of the head coils are interconnected, by a pair of lines called "trunk", into eight groups of 32 with each trunk forming one column of the matrix. Each of the paired lines forming a trunk is connected to a paired write amplifier and preamplifier.

2-13. Quad Write/Preamplifier

There are eight identical Quad Write!Preamplifier circuit cards in the Card Cage Assembly. Four are connected to Disc Spindle Assembly A and the other four connected to Disc Spindle Assembly B. Each Quad Write/Preamplifier (fig. FO-7) contains four identical amplifier/preamplifier channels. Each write amplifier serves a trunk in the Matrix Interconnect circuit card located in the Disc Spindle Assembly. During a write operation, write enable (**WEN**) and trunk select (**TRUNK SEL**) inputs to decoder U2 will remain low. The input of track address 5 (TA5) and track address 6 (TA6) to U2 determines which one of four write amplifiers is selected. The selected write amplifier (i.e., trunk D channel) is enabled by making the set and reset inputs to write amplifier flip-flop U7B high. The encoded write data (**WRITE CLK**) through U7B and gates U8C/D controls current switches Q13 and Q14. The collector of each transistor (TRUNK D) is connected to opposite ends of a readiwrite head coil. The current flow is controlled through each half of the coil, thus establishing polarity of the recorded dipole. The current through Q13 and Q14 is held constant by WRITE CURRENT from the power supply. During read, diode CR54 draws WRITE CURRENT to prevent damage to the current switches. During a read operation, **TRUNK SEL** remains low and **WEN** goes high, inhibiting the four write amplifiers. Inputs TA5 and TA6 to U2 determine which one of four preamplifiers is selected. The selected preamplifier (i.e., trunk D channel) accepts read data from a read/write head on a balanced input line (TRUNK D) through a network required to block the +12 vdc from input to amplifier U10O. Diodes CR41 through CR44 limit voltage during writing prevent damage to U 10 and reduce recovery time. The amplifier is enabled by keeping the base of Q18 at zero volt. This, in turn, gates on the constant current source in U10-2 and provides DATA OUTPUT through CR51 and CR52 to the Data Read Amplifier circuit card.

2-14. Data Read Amplifier

The Data Read Amplifier receives differential analog data from the selected preamplifier and converts the data to NRZ digital format. The differential output of the preamplifier (fig. FO-8) is coupled through transformer T101 to an automatic gain controlled (AGC) analog signal amplifier (U101). Figure 2-5 is a timing diagram for the data read amplifier. The output of U101 is buffered by emitter follower Q102 which drives differential amplifiers Q103 and Q104. These amplifiers are designed to function as an equalizer as required by packing density and disc head frequency response. The output of Q104 is buffered by emitter follower Q105, which drives a three-pole Butterworth lowpass filter comprised of R123, C112, L101, and C113. The output of this filter is buffered by emitter follower Q106.

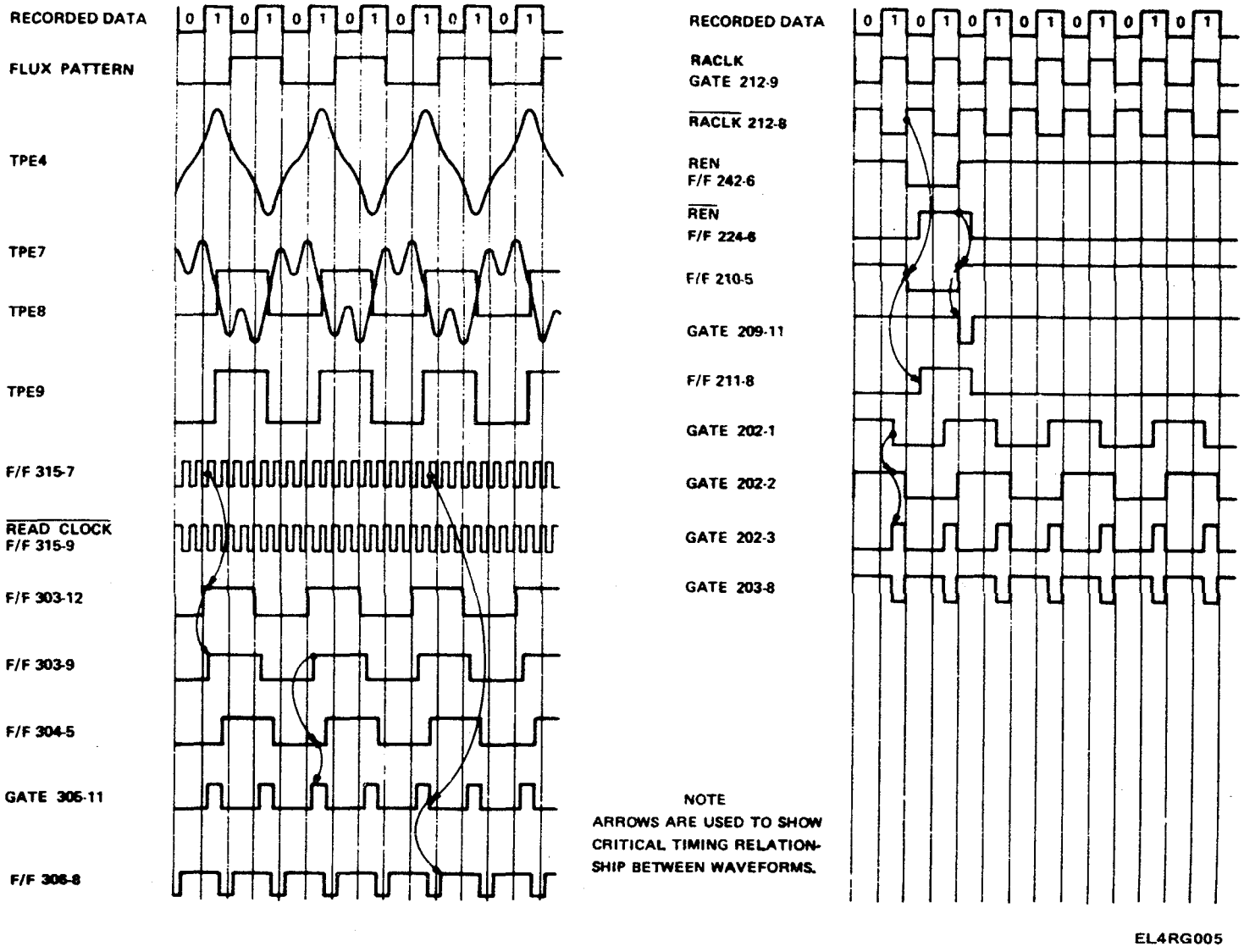


Figure 2-5. Data Read Amplifier Timing Diagram.

a. AGC Loop Gain. The AGC loop gain is controlled by field effect transistor (FET) Q101 that acts as a voltage-variable resistor, which controls the gain to amplifier U101. To accomplish this, dual comparator U103 monitors the output signal from Q106 and compares the positive and negative peak amplitude with fixed reference levels set by voltage dividers R130, R131, R128, and R129. When a signal peak of either polarity exceeds its reference level, U103 produces a positive pulse which drives Q109 to discharge C118 to a lower positive potential. This decrease in positive potential applied to the gate of Q101 causes an increase in the effective Drain-to-Source resistance, decreasing the gain of U101, which in turn reduces the overall loop gain. To reduce noise level in the amplifiers during writing, **AGC RESET** is applied, and drives Q109 to conduction. This causes C118 to discharge through Q109, causing Q101 to decrease the effective Drainto-Source resistance, and, thereby, setting the gain of U101 to minimum. The overall gain is now set to minimum. During write/read, the reference voltage (3.3v) of voltage divider R143, R174 causes U108 to set the gain of amplifier U101 to a fixed level greater than the normal read operate. The analog signal of Q106 is applied to differentiator DL102 and amplifier circuit comprised of U102, Q110 and Q111. The output of Q111 is buffered by emitted follower Q112. The differentiated output signal of Q112 is applied to U103. The output of Q112 is also applied to the threshold zero crossing detection circuits. Threshold detection is used to assure accurate decoding in the proximity of the zero-crossings of the read-back waveform. The threshold detection circuit, basically comparator U104, monitors the Q112 output signal. The U104 output switches high when the amplitude of the input signal is less than the reference voltage applied to the non-inverting input (pin 3), and low when the input signal exceeds the reference voltage. The reference level is developed by feeding back a portion of the output through R166 and R165. Comparator U104 develops a digital output representing the encoded phase-modulated data with a transition occurring at the end of a cell time denoting a logic ONE and a mid-cell or no transition denoting a logic ZERO.

b. NRZ Data. The NRZ data is developed from the output of delay line DL302 by flip-flops U301A/B, and U303B, and gate U205C. Delay line DL302 is driven from PM data detector U104 through gate U203A, delay line DL201, gate U203C, delay line DL301 and gate U203D. The three delay lines are adjusted to align the PM mean time position of data transitions at U301A-12, with the negative transitions of the clock at U301-11. U301A-9 provides a PM output that is synchronized with the read clock. The signal appearing at the output of U301B is lagging the signal at output of U301A by half a cell time. The overlap between these two signals is detected by exclusive OR gate U205C and is applied directly to the input of NRZ restoration U303B, which is clocked by the output of read clock flip-flop U302A.

c. Read Clock. The **READ CLOCK** is developed at pin 9 of flip-flop U302A. **READ CLOCK** is inhibited (held in a zero state) for a selected number of bits (usually two) immediately after **REN** input to flip-flop U211 goes low. Otherwise, the read clock is phase-locked to PM data edges during the read mode when the **REN** signal is low, or to the bit clock during a nonread mode when the **REN** signal is high. The Read Clock control signal (B) appears at the open collector output of gates U202A/B. A low output on this line sets flip-flops U302A and U302B. This low output causes transistor Q305 to conduct, inhibiting the oscillator. When the clock control signal goes high, Q305 ceases to conduct so that the oscillator can operate, and the set line to U302A and U302B is released. When**REN** is applied, a low output from gate U203B is applied to U202B-13. This same output is inverted by U201A and a high signal is applied to gates U202A-10 and U210A-15. The previous high output from U203B loaded shift register U208 with all ONEs. The selected bit (pin 14) of U208 is applied to U202A-9. With U202A-10 driven high, the low output of U202A-+ inhibits the read clock oscillator and counter. PM data from the PM detector U104 drives delay line DL201 through date U203A. Exclusive OR gate U205A provides a positive signal at each data edge by detecting the data overlap at pins 1 and 2. The approximately 1/4-cell time overlap at pins 1 and 2 is controlled by the tap setting of DL201. The overlap determines the edge pulse width.

d. PM Data Edge Pulses. Data edge pulses are fed through U205A as serial clock input to U208-1. As the parallel load control (U208-8) is changed to a low state, the positive transitions of the data edge pulse appearing at pin 1 will cause the forced ZERO state at pin 9, which is the serial data input to be shifted through the register. After two edge pulses, the selected bit will go low and the output of U202A will go high, permitting the read clock oscillator and counter to operate. If the input to U203B goes low, U202A will continue to have a low input due to the selected bit. However, both inputs to U202B are now high; therefore, the read clock is inhibited. The preset signals at flip-flops U204A-4 and U204-B-10 are now high, permitting the forced low input at U204A-2 to be shifted out of U204A-5 on the first positive transition of **RACLK**. When U204A-5 goes

low, the output ot U202B will be driven high, enabling the read clock. Flip-flop U204B-+ goes high two bits after a positive transition in the **REN** signal, occurring when the operating mode is changed from a read to non-read status. This permits the bit clock output of gate U206A to drive reference input R1 and the read clock output of gate U206B Lo drive variable input V1 of phase detector U209A. The output of U210A is held low by the Read Amplifier Enable (REN) signal. Consequently, gates U206C and U206D are able to pass the two outputs of U209A to the corresponding inputs of charge pump U209B. Under these conditions, the read clock will phase-lock to the bit clock. At this time, if **REN** is asserted, U204B-8 will set to a low level, breaking the lock between bit clock and read clock. The phase-locked outputs of U209A are both high and will remain high as long as U206A and U206B remain inhibited. Consequently, U206C and U206D now pass outputs of the data edge phase detector, comprised of gates U207C and U207D, to U209B. The first data edge, after **READ CLOCK** control signal goes high, will be gated out by the phase-detector input (U303A). However, the first edge pulse sets the output of U303A high so that succeeding edges are gated through U210A and inverter U201C to the data edge phase detector.

e. Data Edge Phase-Locking. When the read clock is phase-locked to the data edge, the data edge pulse will be centered about the negative-going transition of the Read Clock signal. Thus, at lock-on, equal area pulses will appear at the charge pump up (PU) and down (PD) inputs. However, they will be slightly displaced in time with the trailing edge of the pump down signal approximately in line with the leading edge of the pump up signal. Fixed propagation delays produce a time lag between the release of the Read Clock Inhibit line and the first clock pulse; therefore, DL202 is set to align the data edge pulse initially with the clock so that large errors will not have to be removed by the fairly slow response loop.

f. Phase Error. The phase error pulses from charge pump U209B have precise levels, and the pulse width depends upon phase error. These pulses are coupled to the summing junction of the filter amplifier through R301 and R302. The filter amplifier is comprised of R301, R302, R303, R307, C301, C308, Q301 and Q302. This amplifier integrates the phase error pulses and produces a dc output of the correct level to drive the voltage-controlled relaxation oscillator at the correct frequency. An emitter follower Q303 is used to drive current source transistor Q304. The base of Q304 is held at approximately +3.3v by R304 and R305 acting as a voltage divider. The emitter of Q304 is held at approximately +4v by R310. The dynamic operating voltage range at the emitter of Q303 (TPE5) is from +4.5v to approximately +9v. Resistor R310 sets the lowest frequency at which the clock can run by setting the maximum Q304 emitter current to approximately 1/2 ma. The frequency is determined primarily by how much time it takes the current source transistor to charge C305 up to the threshold level of Q308. The base of Q309 is held just slightly above two volts when Q308 is not conducting. The collector current of Q309 produces a voltage drop across R313 and drives the base of 0307 negative with respect to its emitter, causing Q307 to conduct. The collector current of Q307 produces a voltage drop across R312 and drives the base of Q306 positive with respect to its emitter so that Q306 is held in the off state. The emitters of Q308 and Q309 are set at slightly under two volts. When the base of Q308 reaches the turn-on level, it drives Q309 off by reducing the base drive through CR304, CR305, and CR306. When Q309 turns off, it causes Q307 to turn off and Q306 to turn on. The conduction of Q306 discharges C305. The emitter of Q308 will follow the base voltage as it is driven downward by the discharge of C305. When the emitter of Q309 is driven below its new base level, Q309 will turn on and drive Q308 off. Diodes CR302 and CR303 prevent Q307 from going into saturation, thus decreasing switching time.

2-15. Clock Amplifier

There are two identical clock amplifier circuit cards in the Card Cage Assembly. One card serves Disc Spindle Assembly A and the other serves Disc Spindle Assembly B. The Clock Amplifier circuit card receives the Ferranti-encoded analog signal from the clock head, converts the information to a symmetrical clock pulse train of two times the record clock frequency, and develops the origin pulse or index clock signal that marks the beginning of each disc revolution. This amplifier employs a dual detection technique that effectively blanks out the input waveform in the proximity of the zerocrossings. This method of detection enhances decoding accuracy by inhibiting the detection of a single transition unless the reversal is anticipated. The recorded clock tracks are read by clock head 1A and 2A.

a. Clock Head Selection. The position of clock head select switch S101 allows either clock head to be utilized (fig. FO-9). The analog signal from the clock head is applied to balanced differential amplifier U101 whose output is applied to a conventional wide-band amplifier U102. The output of U102 passes through a low-pass filter (R110, R111,

C108 and C116) and is buffered by emitter follower Q101. The output of Q101 which copies the output signal of U102 is applied to peak and threshold detection circuits. Peak detector/comparator U103 monitors signal cross-overs of the Q101 output, switching low for each positive transition and high for a negative transition. This output of U103, a digital signal representing each transition of the input analog signal, is dropped across R119 and applied to the summing node input of high-speed comparator U113. The threshold detector, comparator U104, monitors the Q101 signal. A portion of U104 output is fed back through R123 and R124 to its non-inverting input pin 3. When the amplitude of the signal input to the inverting inputs goes lower than the feedback reference level, U104 switches to provide a high output. This causes the feedback reference level to increase to a value greater than the zero-crossing value, and, as the input signal swings positive, U104 is not switched low until the amplitude exceeds the zero-crossing level. In this manner, the signal transitions are sensed by the threshold detector with the positive slopes developing a low U104 output and the negative slopes a high output. The output of U104 is dropped across R126 and applied to the summing node input of data detector U113. The magnitude of the threshold detector output signal is not high enough to switch U113. The combined output from the peak and the threshold detection circuits is required to initiate a change in the state of U113. Detector U113 monitors the combined signal from the peak and threshold detection circuits and is switched only when U103 and U104 are in the same state. That is, if peak detector U103 denotes a positive signal transition and threshold detector U104 has not sensed the negative slope, then the amplitude of the U113 input at the summing node is less than the feedback reference signal to U113-3 and U113 remains in the high state. Detector U113 is switched when U104 senses the occurrence of signal transition. The U113 output (TPE3) is a Ferranti-encoded digital signal representing the recorded clock track.

b. Digital Output. The digital output of the clock read amplifier at detector U113-9 (fig. 2-6) has a single half-frequency cycle in an otherwise continuous full-frequency clock pattern used to establish an orientation reference needed in the sector address function. Note that the positive period of the half-frequency cycle appears first. This signal is inverted by gate U106A and is connected to the reference input (R1) terminal of phase detector U105A. When the circuit is phase-locked, the negative-going transitions of the reference and variable inputs of phase detector U105A will be in alignment. If the variable input is lower in frequency or lags in phase, the up output goes low; conversely, if the variable input is higher in frequency or leads in phase, the down output goes low. The duty cycles of the two signals are not important, only the alignment of the negative transitions. The two outputs of U105A are connected to charge pump inputs PU and PD. The charge pump U105B converts these signals to fixed amplitude pulses. The voltage appearing at the DF output should be approximately +1.5v in a pump down state. When not in a pump down state, the DF output should be an open circuit. The UF output should be about '+0.5v when in a pump up state. Otherwise, the UF output should be an open circuit. The DF and UF outputs of the charge pump are connected through resistors R134 and R135 respectively, to the summing junction of filter amplifier U105C. The output of U105C is also fed back to its summing junction through resistor R136 and capacitor C118. Charge pump U105B and U105 C share a +5v power supply which is comprised of resistor R137 and Zener diode VR101. A decoupling network (R138, C117 and C132) prevent the filter amplifier from interfering with the charge pump.

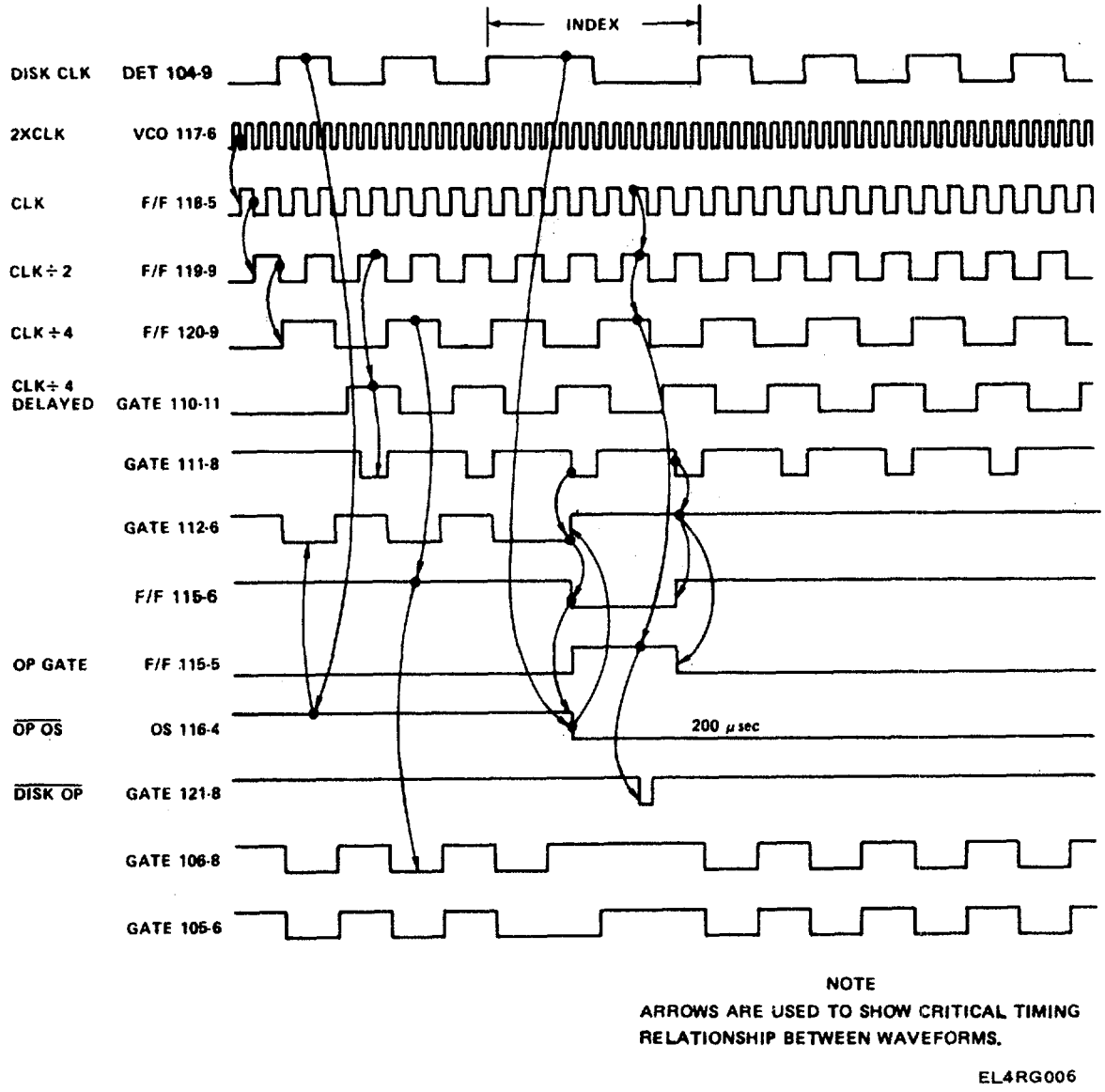


Figure 2-6. Clock Amplifier Timing Diagram.

c. Voltage Control. The output of U105C is coupled through a low pass filter network (R139 and C119) to the voltage control oscillator (VCO) U108. VCO U108 has its own power supply (resistor R140, Zener diode VR102, and capacitors C121 and C122). Counter U109A is driven directly from U108 and produces a symmetrical clock that is two times the recorded frequency. Clock (CLK) is produced by U109A and is used as a phase-lock reference for the read clock phase detector during a non-read mode. Counter U109B produces a $\frac{CLK}{2}$ output. Counter U110B is driven from U109B and produces a $\frac{CLK}{4}$ output used to drive gates U106B, U106D and U111A. Gate U111A receives inputs from U110A-5, U11OB-9, U109A-5 and U109B-9 to produce DISK OP. Gate U106B receives inputs from U110-9 and U110A-6, and produces, at its output, the variable input reference (V1). The continuous square wave signal at the output of U110B has a single zero state period changed to a one state at DISK OP time by U106B and U11A. The resulting signal that is produced at the phase detector U105A variable input (V1) has the same number of negative transitions as the Ferranti clock signal and ensures a stability of the phase-lock circuitry. Gate U106B complements the signal from U106B-9 and drives delay line DL102 which delays the signal 50 nanoseconds. Gate U107A receives signals from DL102 and U109B-9 and produces at its output a strobe signal for U11A.

(1) BCN. Bit count n (n = 2, 4, 10, 14 and 16) is a one-bit wide pulse occurring during the nth bit time of every word during every revolution of the disc. When the disc is ready, and during disc origin pulse time, the outputs of bit counter U201 are forced low for initialization. Then the counter starts to count the recorded clock pulses from the disc. The binary output is decoded by U202 into decimal outputs **BC2**, **4, 10, 14, 16**. **BC2** and **BC10** are sent to the Control Logic circuit card. **BC4** is ANDed with **WRD1** to develop SECT STRB. **BC14** is used to check for clock errors. **BC16** (one word) is applied to word counter U203.

(2) WC53. Word count 53 is developed by word counter U203 and U204. At the start of every sector, counter U203 is initialized to a count of 12. Therefore, counter U204-6 is WC53 instead of WC64. WC53 is used to determine the end of DT within each sector. WC53 is also sent to the Control Logic circuit card.

(3) **WRD1**. Word one is a 16-bit wide pulse occurring during the first word of every sector. When disc is ready and disc origin pulse time (DISK RDY.DISK OP) sets, word one flip-flop U208A sets, and WRD1 is applied). Disc origin pulse (**DISK OP**), which is a one-bit wide pulse, occurs only at sector zero. **DISK OP** sets U208A, applying **WRD1**. Counter U202 counts up to 15; the **BC16** output triggers U208A, causing Q output to go low; and **WRD1** terminates. At the end of the sector WC61 (1/2-bit wide pulse) is developed and applied to the reset flip-flop U207A. **RST** is generated and applied to one input of gate U209A. **RST** sets U208A, generating **WRD1** of sector one. Counter U201 counts up to 31; Q output of U208A goes low; and **WRD1** terminates. **RST** asserts **WRD1** of sectors 1 through 90.

(4) DT. Data time is a level which begins after BC10 of the second word and ends after BC10 of the 53rd word of every sector. DT defines the period during bus write data (BWD) is being written on the disc. When disc is ready or no origin pulse or no reset pulse is present, **WRD1** (Q output of word one flip-flop U208A) is low and ANDed with WC53, whose product is applied to the dat time flip-flop U208B to develop DT.

(5) DISK RDY. **DISK OP**. **RST**. Disc ready and disc origin pulse and reset is a term used to initialize counters and flip-flops on the Control Logic circuit card. This line is low when the disc is not ready or during origin pulse or reset pulse. Whenever this line goes low, data time flip-flop U208B resets and DT goes low.

(6) SECT STRB. Sector strobe is a one-bit wide pulse which occurs during **BC4** of **WRD1** of every sector.

(7) **SECT CLK**. Sector clock is a one-bit wide pulse which occurs during **BC10** of **WRD1** of each sector except sector zero. During sector zero, gate U107A is disabled by **OP OS**.

(8) OP. Origin pulse is a one-bit wide pulse which occurs during **BC10** or **WRD1** of sector zero. During sectors 1 through 90, gate U209C is disabled by OP OS.

(9) **DISK RDY**. Disc ready goes low following **DISK OP** if no clock errors exist (**CLK ER** high), power supply is ready (**PS RDY**), and cable connector interlock (**INT LK RDY**) completed. With the above condition, a high level signal is applied to DISK RDY flip-flop U207B, whlch is clocked by **DISK OP**. The high Q output is inverted and sent to the Control Logic circuit card. The high Q output is also ORed with **DISK OP** to develop **DISK RDY** + DISK OP and DISK RDY. **DISK OP**.

(10) **SECTOR ADDRESS LINE 0** through **6**. The sector address lines 0 through 6 transmit to the RASC, in binary form, the sector (1 of 91) being addressed. DISK OP forces all the outputs of counter U303 and U304 to go low, indicating sector zero. At the end of every sector except the last

sector (90th), word count WC61 (1/2-bit) is developed. WC61 is applied to CLK input of counter U303. Counters U303 and U304 count up to 90; get cleared by DISK OP; and are reinitiated by WC61. **DISK SEL** low enables sector address gates.

(11) RECV OS. Recovery one-shot U303 goes low 55 ms after disk is ready. The low **Q** output of DISK RDY flip-flop U207B is applied to the B input of U301A. U301A is triggered by **DISK OP** and its **Q** output (high level) is inverted and sent to the Control Logic circuit card. If disc is not ready, the B input of U301A goes high and its Q output goes low.

(12) CLK ER. Clock error is applied whenever DISK OP is not detected within one disc revolution, or if OP GATE occurs during **BC14** (high). Any of these conditions will cause the input to gate U212D to go high. CLK ER is sent to the Control Logic circuit card.

(13) **CLR**. Clear from the Control Logic circuit card causes flip-flop U302A and U302B to set, driving their **Q** outputs low and removing CLK ER. The retriggerable one-shot U301B is triggered by DISK OP. Its **Q** output (low level) is slightly longer than one revolution; therefore, **Q** output remains low. This low level signal is used to clock U302A. The **Q** output of U302A remains low as long as DISK OP is detected within each revolution. When disc is ready and at **BC14** time, the input to U302B goes high and at that instant, OP GATE triggers the flip-flop, keeping its **Q** output low. The **Q** output will remain as long as **BC14** and OP GATE are in sync.

2-16. Control Logic

The Control logic circuit card implements Read Enable and Write Enable commands; encodes input data for writing; concurrently superimposing preamble, postamble, and gap timing format, stripping this format from data being read; and interfaces with Clock Amplifier circuit card in generating timing signals (fig. FO-10).

a. PARITY ERROR. Parity error is a low active signal detected by parity error flip-flop U212A. Upon detection of parity error, the RAS will transmit a low active signal to the RASC. **RAS SEL** enables gates U309A through U309D.

b. CLOCK ERROR. Clock error is a low active signal detected in the Clock Amplifier circuit card. CLK ER is routed through multiplexer U112 to gate U309C. Upon detection of clock error. the RAS will terminate operation and transmit a low active signal to the RASC.

c. READ DATA. Read data RD from the Data Read Amplifier circuit card is inverted by gate U309A and sent to the RASC. A low active signal indicates a logic 1 has been read.

d. W/R CLK. The low active write/read clock signal is sent to the RASC when data is being transferred during a read or write operation. During a read or write operation, gates U204A or U204B will be enabled, respectively, allowing W/R CLK to be developed. A sync bit is inserted in the read and write clock stream after every 8th bit (fig. 2-2). Counter U209 counts **DATA CLK** and at the 8th bit sets sync flip-flop U213A. **SYNC** is applied for one-bit time, disabling gate U105B and creating a gap 1.5-bits wide in the clock stream.

e. MASTER CLOCK, INDEX CLOCK, SECTOR CLOCK and SECTOR ADDRESS STROBE. The low active master clock, index clock, sector clock, and sector address strobe are sent to the RASC. Clock (**CLK**), origin pulse (OP), sector clock (**SECT CLK**), and sector strobe (SECT STRB) from the Clock Amplifier circuit card are routed through multiplexer U114 to gates U310A through U310D, which are enabled by DISK CHANGE.

f. WCLK-1, -2, -3 and -4. Write clock **WCLK-1** through **WCLK-4** are sent to the Quad Write/Preamplifier circuit card. **WCLK-1** through **WCLK-4** are developed by write clock flip-flop U304A when gates U301A or U301B are enabled or SYNC is applied. BWD (**WRITE DATA**) is one of the inputs to U301A. CLK enables gates U305A through U305D. During read operation, WEN goes low and resets U304A, disabling U305A through U305D.

g. WEN-1 and WEN-2. Write enable **WEN 1** and **WEN 2** are sent to the Quad Write/Preamplifier circuit card. During a write operation BWEN (**WRITE ENABLE**) is generated and applied to the write enable flip-flop U304B. The Q output (WEN) is developed into **WEN-1** and **WEN-2**.

h. CLR. The clear signal is generated when **ERROR RESET** interface line is low. **CLR** sets parity error flip-flop U212A, causing the **Q** output PAR ER to go low. The output of gate U309D goes high and the selected RAS resumes operation. **CLR** is also sent to the Clock Amplifier circuit card to inhibit CLK ER.

i. DISK SEL A and DISK SEL B. Disc select A and B are generated by gates U203B and U203A, respectively. Either A or B is generated at any one time and sent to the Clock Amplifier circuit card. RAS SEL from the RASC enables U203A and U203B. Track address TA9 high selects U203A and allows multiplexers U112, U113, and U114 to select inputs from Drive B Clock Amplifier. TA9 low selects gate U203B and allows U112, U113, and Ul14 to select inputs from Drive A Clock Amplifier.

j. DISK A OK and DISK B OK. Disc A and B okay signals are sent to the Interface Logic circuit card. **DISK A OK** is generated when **DISK A RDY**

and RECV OS A inputs to gate U103B are low. **DISK B OK** is generated when **DISK B RDY** and RECV OS B inputs to gate U103C are low.

k. EN SEL AND AGC RESET. Enable select is generated during read or write and sent to the Interface Logic circuit card. During write, the **Q** output of the write enable flip-flop U304B allows **EN SEL** to be applied. During read, the **Q** output of the AGC reset flip-flop U308B allows **EN SEL** and AGC RESET to be applied. AGC RESET is sent to the Data Read Amplifier circuit card.

l. REN. During a read operation, the low level BREN (**READ ENABLE**) is applied to read enable flip-flop U208A, whose Q output is ANDed with **WRD1**. Read enable (**REN**) is sent to the Data Read Amplifier circuit card. During a write operation, U208A is reset and **REN** is held high.

m. RA CLK. The read amplifier clock is a symmetrical clock pulse train derived from CLK of the selected Clock Amplifier. With both disc A and B ready (**DISK A RDY** and **DISK B RDY** low) and TA9 high, gate U107D (bottom) allows **CLK B** to develop **RA CLK**. When TA9 goes low, gate U107D (top) allows **CLK A** to develop **RA CLK**. The **RA CLK** is inverted and send to the Data Read Amplifier circuit card via gate U203D.

n. SEQ DN. The sequence down signal is generated by gate U103A when both **AC FAIL** and WEN signals go low. This low level signal is sent back to the Power Supply Assembly where it disables **DC PWR READY** signal; the RAS then goes off line. WEN is developed through the Q output of write enable flip-flop U304B when BWEN (**WRITE ENABLE**) interface line is low during a write operation.

o. RDY LMP A and RDY LMP B. When Disc Spindle Assemblies A and B are both ready (**DISK A RDY** and **DISK B RDY** low), motor cables W1, W2 are connected, and RDY LAMP A and B (+12v) are applied to DISK READY A and B lamps on the front panel, indicating that discs A and B are ready. The DISK READY A and B lamps may be tested by depressing LAMP TEST switch on the front panel after the power supply has sequenced to the ON condition.

p. INIT and INIT-1. Initialize is applied through gates U205C and U211B when disc is not ready, when the disc OP occurs, and during reset or when the RAS is not selected. **INIT** allows counter U209 to set its outputs, and resets read enable flip-flop U208A. **INIT-1** resets flip-flops U213A, U208B and U213B; sets flip-flop U212B; and forces the CARRY output of counter U210 to go low.

2-17. Power Supply.

AC power (115v, 60 Hz, single-phase) is applied to connector J1 (FO-11); filtered by FL1 and FL2; and applied to transformer T1 across switch CB1. One secondary output of transformer T1 is connected to a full-wave bridge rectifier CR1, whose output is filtered + 10v. The center tapped secondary of transformer T1 is connected to a fullwave bridge rectifier CR2, whose outputs are filtered +17v and -17v. The center tapped secondary is also connected to a halfwave bridge rectifier CR101 and CR102, whose output is +AC SENSE signal. An elapsed time meter M1 records the number of hours the RAS has been on line. Relay K2 energizes and stays energized for approximately 30 seconds, during which time both disc spindle drive motors have been started and brought up to speed. During the first 15 seconds, relay K1 remains deenergized, allowing drive motor "B" to start up. Then K1 energizes and allows drive motor "A" to start up. After both drive motors have been started and brought up to speed (approximately 30 seconds), K2 deenergizes. Relay K1 is held energized until ac power is removed.

a. AC Undervoltage Detection. The +AC SENSE is a dc voltage developed by half-wave bridge rectifier CR101 and CR102. This dc voltage is dropped across voltage divider resistors R316, R317, and R318. The base voltage of transistor Q305 is held slightly higher than the emitter voltage (+5.1v). The positive emitter base voltage holds Q305 off, maintaining the base of Q306 at ground level, keeping Q306 off. The collector of Q306 rises o +5.lv, causing gate U501B-8 to go high and allowing PWR (DS1) indicator to light. Gate U501C-8 is also high (**AC FAIL**) which causes gate U403C-11 to be high, keeping UNDER SPEED (DS3) indicator off. The **AC FAIL** from connector J2-P is jumpered to J2-R as **SEQ DN**. The **SEQ DN** signal being high causes the input to gates U506A-4, U506B-14, and U502B-9 to be high, thereby developing a condition to develop control signals for sequencing. The low level +WV CROWBAR signal from gate U504B-12 is applied to diode CR201. If ac should fail or drop to 85 percent or less than normal, +WV CROWBAR goes high and fires thyristor Q9, shunting + WV (+ 12v) to ground, and the RAS initiates a dc power down sequence.

b. Disc Spindle Power Up Sequencing. Disc spindle power up sequencing occurs during time To through T3 (fig. 2-7).

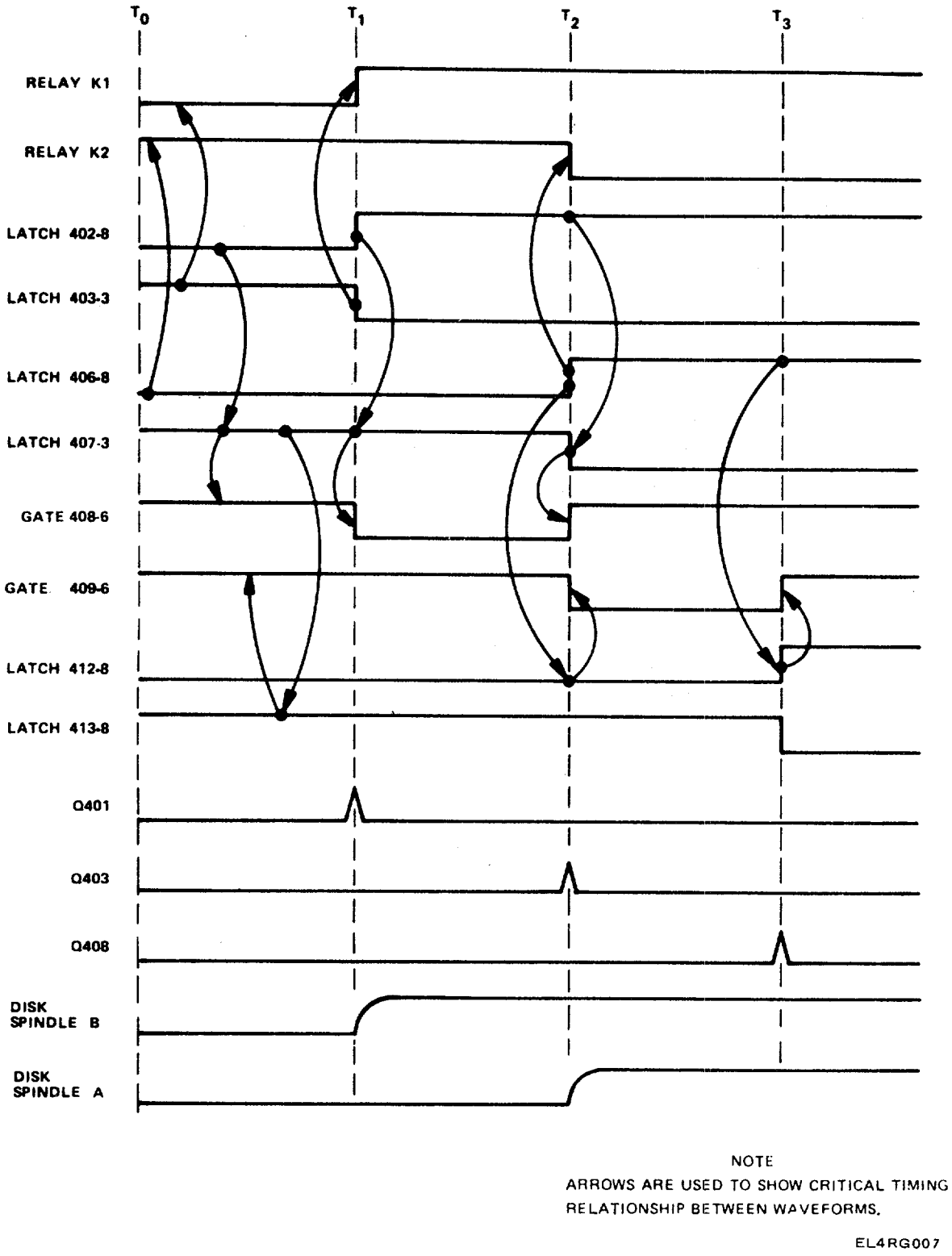


Figure 2-7. Disc Spindle Power Up Sequencing Timing Diagram.

When switch CB1 is initially turned ON at a time TO, the following sequence of events occur:

(1) All three latches (U401B/U401C, V402B/V402C, and U403B/U404A) are reset.

(2) Relay K2 energized.

(3) Disc spindle "B" powers up.

(4) Transistors Q404 and Q407 conduct, disabling unijunction transistors Q403 and R408, respectively.

(5) Transistor Q402 is held off, allowing capacitor C401 to charge and raise the emitter voltage of unijunction transistor Q401.

(6) At the time T1, the emitter voltage of Q401 reaches + 9v.

(7) Transistor Q401 conducts.

(8) Latch U401B/U401C sets.

(9) Transistor Q402 conducts, and turns off transistor Q401.

(10) Relay K1 energizes.

(11) Disc spindle "A" powers up.

(12) Transistor Q404 is held off, allowing capacitor C402 to charge and raise the emitter voltage of unijunction transitor Q403.

(13) At time T_2, the emitter voltage of Q403 reaches +9v.

(14) Transistor Q403 conducts.

(15) Latch U402B/U402C sets.

(16) Relay K2 deenergizes.

(17) Transistor Q404 conducts, and turns off transistor Q403.

(18) Transistor Q407 is held off, allowing capacitor C403 to charge and raise the emitter voltage of unijunction transistor Q408.

(19) At time T3, the emitter voltage of Q408 reaches +9v.

(20) Transistor Q408 conducts.

(21) Latch U403B/U404A sets.

(22) Transistor Q407 conducts, and turns off transistor Q408.

(23) Output DCON of latch U403B/U404A is high.

c. DC Voltage Sequencing. The dc voltage sequencing is accomplished during time T3 (fig. 2-8). The control voltages are developed to turn on dc voltage regulators, and at time T3, DCON is applied and the following events occur: (1) The +12v, +5v and -12v CONTROL signal levels are developed.

(2) The +WV CONTROL signal level is developed.

(3) **DC PWR READY** is applied.

(4) After approximately 125 ms, latch U503B/U506A will set and reset during the time gate U505A-8 goes negative and positive.

(5) Any of the inputs to gate U506B going low will cause DC PWR FAULT (DS4) to light and **DC PWR READY** signal to go high. The **DC PWR READY** signal is sent to the Clock Amplifier circuit card. If temperature rises to a level where thermostat S2 opens, the following events occur:

(6) Lose +WV

(7) Lose +12v, +5v, and -12v.

(8) DC PWR FAULT (DS4) and OVERTEMP (DS2) indicators light.

(9) RAS powers down.

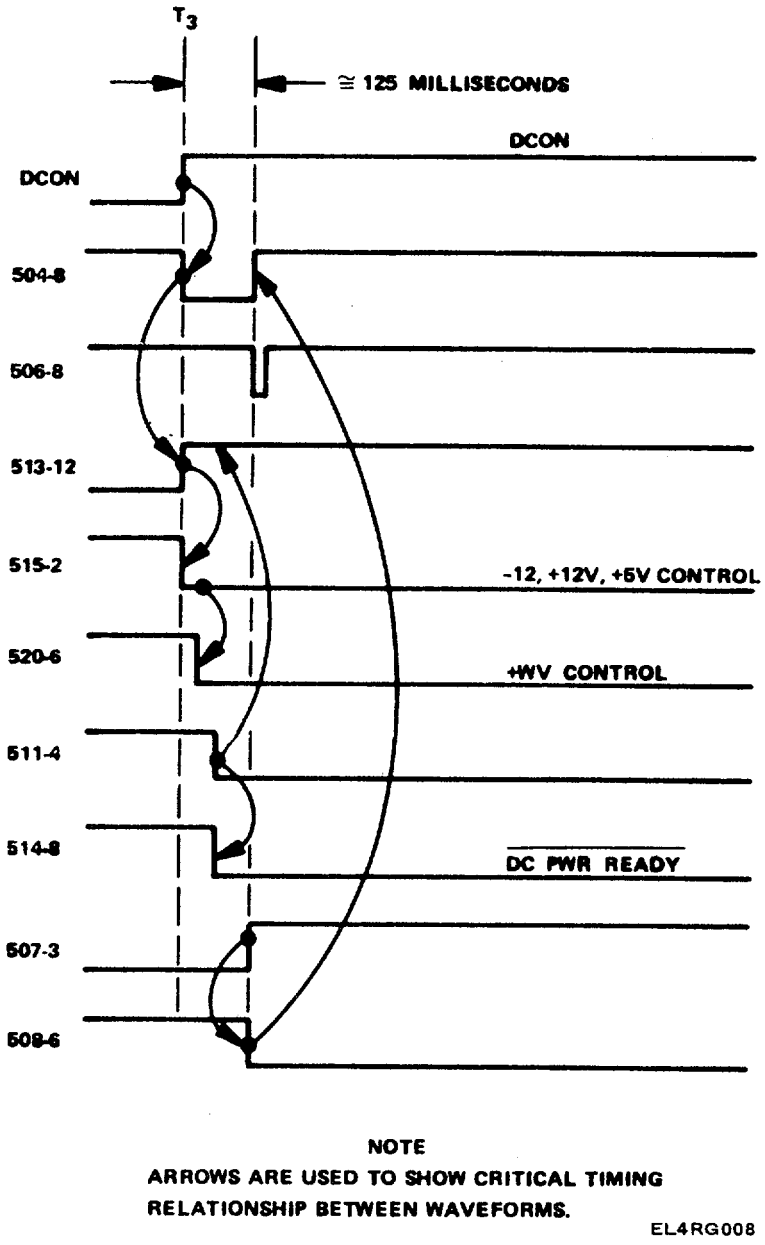


Figure 2-8. DC Voltage Sequencing Timing Diagram.

d. Voltage Regulation. The voltage regulation for the +12v, -12v, +5v and +WV are similar; therefore, only the +12v voltage regulator will be covered. Voltage regulator U203 regulates the amount of voltage dropped across series pass transistor Q205. Thyristor Q2 and Zenor diode VR202 make up the overvoltage protection circuit. Transistor Q206 controls (disable or enable) regulator U203. When the control signal at the base of Q206 is high, Q206 conducts, applying ground potential to U203-13. The regulator senses the ground potential and transistor Q205 is biased off. When the control signal at the base of Q206 goes low, Q206 switches off, removing ground potential from regulator U203-13; and allowing Q205 to conduct. The output voltage is sampled at the junction of resistors R217 and R218. If the sampled voltage is greater than +12v, the bias on Q205 is decreased, causing a decrease in voltage drop across Q5. If the sampled voltage is less than +12v, the bias on Q205 is increased, causing an increase in voltage drop across Q205. Varying the bias to Q205 regulates the voltage dropped across Q205.

CHAPTER 3

DIRECT SUPPORT MAINTENANCE INSTRUCTIONS

Section I. GENERAL

This chapter provides direct support maintenance instructions for the RAS. Direct support maintenance is performed by acitivites designated to support the using organization, and emphasizes corrective maintenance at the equipment site.

Direct support maintenance is performed on items identified as faulty at the organizational level, but require skills and training to affect repair that is beyond the skills and training of organizational level personnel.

Section II. TOOLS AND EQUIPMENT

3-1. Tools and Test Equipment.

Tools and test equipment required to perform the maintenance procedures given in this chapter are listed in table 3-1. The test equipment listed in table 3-1 is authorized for use by direct support personnel. Any tools or test equipment authorized for use at the organizational level are also authorized for use at the direct support level.

3-2. Repair Parts

Repair parts and accessories authorized for use by direct support maintenance for the RAS are listed in the Repair Parts and Special Tools List (TM 11-5895-860-34P).

Table 3-1. Tools and Equipment

Item	Purpose
Torque Wrench, zero to 30 in-lb range, with hexagonal key adapters for socket head screws and screwdriver adapaters for cross-recessed screws, Numbers 1 and 2 sizes.	Removal of card cage assembly.
Handle, Socket Wrench, 1/4 inch square drive socket holder; ratcheting.	Removal of: a. Handle. b. Slide.
Socket, Socket Wrench: double hex (12-point); 1/4-inch square drive; regular length; 5/16-inch nominal opening; Fed Spec GGG-W-641, Type II, Class 2. Style A.	Removal of slide.
Socket, Socket Wrench: double hex (12-point); 1/4-inch square drive; regular lenght; 9/16-inch nominal opening; Fed Spec GGG-W-641, Type II, Class 2, Style A.	Removal of handle.
Screwdriver: cross tip; straight; plastic handle; number 2 point size; 4-inch nominal blade long; Fed Spec GGG-S-121, Type VI, Class 1, Style 1.	Removal of: a. Card cage assembly. b. Front panel assembly. c. Power supply assembly.
Multimeter AN/USM-233	Checking cable assemblies and circuit card dc voltages.
Card extender 11160 ASSY 05-035-926-01 (fig. 3-1)	Allow circuit card to be extended for checks.
Oscilloscope AN/USM-281C oscilloscope, plug-in.	Troubleshooting.
Wire Wrap Tool Kit.	Repair of card cage assembly.

Section III. TROUBLESHOOTING

3-3. General

The troubleshooting procedure in table 3-2 lists the malfunctions, probable causes, and corrective actions for replaceable items within the RAS unit at the direct support maintenance level. The troubleshooting procedure is based on the condition that organization level troubleshooting has been performed and that circuit cards and assemblies replaceable at the organizational level are operating properly. Once the fault has been determined, refer

to the removal and replacement procedures in Section IV of this Chapter.

a. Extraction of Circuit Cards from Card Cage. Each circuit card location in the card cage has upper and lower locking tabs on the card cage rail. To free the circuit card for extraction, these tabs must be extended outward until they are parallel with the card cage rail. Each circuit card also has an upper and lower tab. When these tabs are extended outward, they separate the card from the card cage connector and the card can then be removed.

b. Insertion of Circuit Cards in Card Cage. Before inserting the circuit card in the card cage, place the upper and lower tabs in the "home" position. The card may then be inserted. As the card starts to engage the card edge connector, firmly drive the circuit card home. Close down the card cage locking tabs.

CAUTION

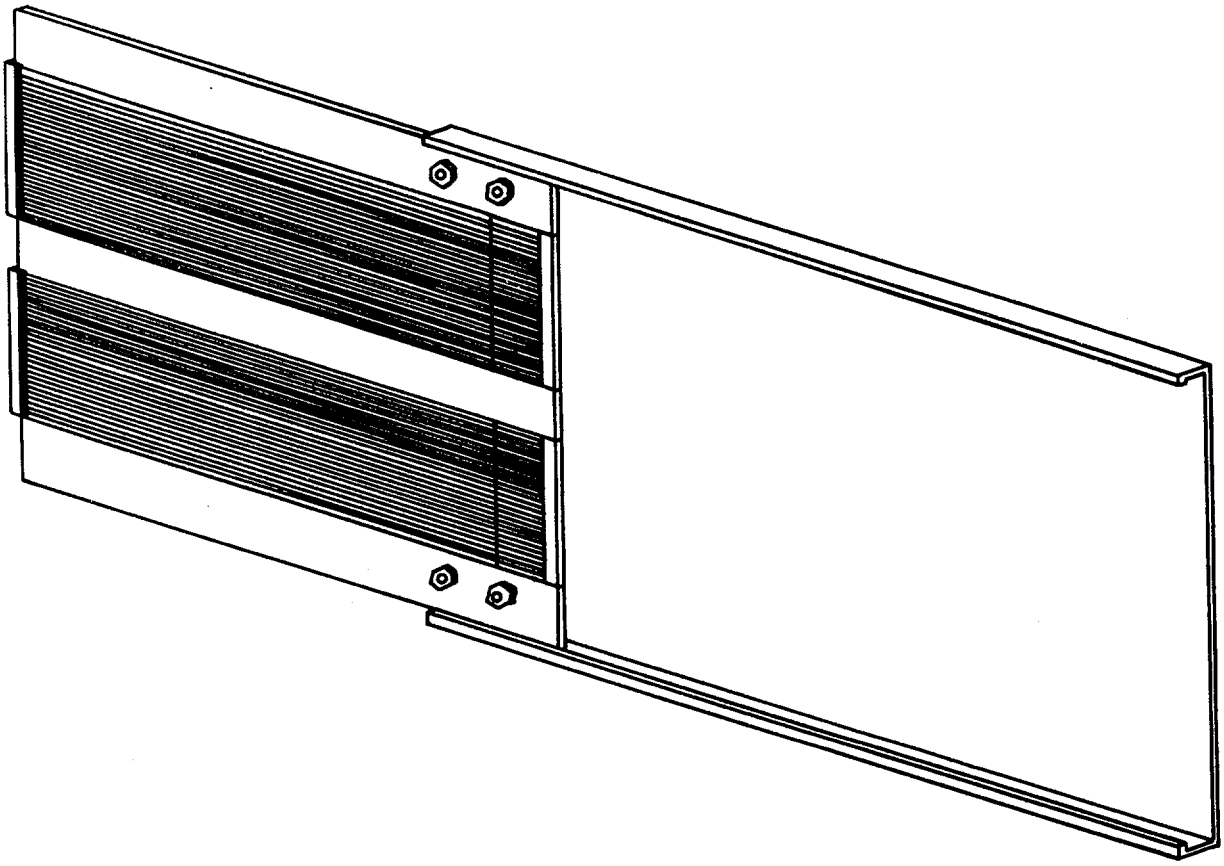
To ensure a stable and secure mating of the circuit card with the card cage connector, the tabs on the card cage connector must be in the locked position.

c. Circuit Card Operating Voltages. The operating voltages for the circuit cards can be checked using multimeter AN/USM-233 and the card extender (located in maintenance shelter) shown in figure 3-1. The operating voltages for the circuit cards are as follows:

J10 through J26	*Voltage*
pin 24	+5 vdc
pin 26	+ 12 vdc
pin 28	-12 vdc

CAUTION

Turn off power to the RAS before removing or installing circuit cards.



EL4RG009

Figure 3-1. Card Extender.

d. Repair. Repair of the RAS is limited to the following:

(1) Replacement of circuit cards.

(2) Replacement of disc spindle assemblies.

(3) Repair and replacement of card cage assembly.

(4) Repair and replacement of interconnecting cables.

(5) Repair and replacement of power supply assembly.

Table 3-2. RAS Troubleshooting

Malfunction	Probable cause	Corrective action
Card replacement fails to correct fault related to the following and in fault catalog:		
J10	a. Cable W4, W5, W8 or W9	a. Repair or replace cable W4, W5, W8 or W9
	b. Card cage assembly	b. Repair or replace card cage assembly
J 11	a. Cable W4, W5, W8 or W9	a. Repair or replace cable W4, W5, W8 or W9
	b. Card cage assembly	b. Repair or replace card cage assembly
J12	a. Cable W8	a. Repair or replace cable W8
	b. Card cage assembly	b. Repair or replace card cage assembly
J13	a. Cable W8	a. Repair or replace cable W8
	b. Card cage assembly	b. Repair or replace card cage assembly
J14	a. Cable W5	a. Repair or replace cable W5
	b. Card cage assembly	b. Repair or replace card cage assembly
J15	a. Cable W5	a. Repair or replace cable W5
	b. Card cage assembly	b. Repair or replace card cage assembly
J16	a. Cable W4	a. Repair or replace cable W4
	b. Card cage assembly	b. Repair or replace card cage assembly
J17	a. Cable W4	a. Repair or replace cable W4
	b. Card cage assembly	b. Repair or replace card cage assembly
J18	Card cage assembly	Repair or replace card cage assembly
J19	a. Cable W4, W5, W8 or W9	a. Repair or replace cable W4, V5, W8 or W9
	b. Card cage assembly	b. Repair or replace card cage assembly
J20	a. Cable W7	a. Repair or replace cable W7
	b. Card cage assembly	b. Repair or replace card cage assembly
J21	a. Cable W3 or W7	a. Repair or replace cable W3 or W7
	b. Card cage assembly	b. Repair or replace card cage assembly
J22	a. Cable W8 or W9	a. Repair or replace cable W8 or W9
	b. Card cage assembly	b. Repair or replace card cage assembly
J23	a. Cable W4 or W5	a. Repair or replace cable W4 or W5
	b. Card cage assembly	b. Repair or replace card cage assembly
J24	a. System interface cable A1J2 or A1J3	a. Repair or replace system interface cable A1J2 or A1J3
	b. Card cage assembly	b. Repair or replace card cage assembly
J26	a. System interface cable A1J2 or A1J3	a. Repair or replace system interface cable A1J2 or A1J3
	b. Card cage assembly	b. Repair or replace card cage assembly

3-4. Voltage and Resistance Measurements

Voltage, resistance, and continuity measurements are made by direct support maintenance for troubleshooting faults which cannot be resolved or repaired by organizational level maintenance. Normally such faults are traceable to wiring or chassis-mounted components. Use the wire run lists (tables 3-3 through 3-5) and foldout diagrams (figure FO-1 through figure FO-16 to support troubleshooting. Data in table 3-3 is arranged in alphabetical sequence of the signal names used on foldouts. Not all signal connections appearing on foldouts are used, and may not appear in wire run lists. The data in table 3-4 is arranged in alphanumeric sequence by jack numbers. Table 3-5 refers to the disc assembly itself. All input and output signal connections shown on foldouts may not be used. Signal connections that are not used do not appear in the wire run lists.

3-5. Matrix Board Maintenance

The matrix boards mounted on the component side of the Spare Track Select Logic (A or B) cards are removed from the logic cards during sparing to facilitate soldering. If damaged, the matrix boards are replaced with new ones and jump-wired to the same configuration.

3-6. Card Cage Maintenance

Two types of card cage repair can be done at the direct support maintenance level: wire replacement and connector pin removal and replacement. Wire replacement instructions for the card edge connector are given in paragraph 3-19. When removing and replacing a card edge connector pin, refer to the point-to-point wire lists in tables 3-3 and 3-4.

3-7. Interconnecting Cable Maintenance

The direct support maintenance of the interconnecting cables involves the removal and replacement of connector pins.

3-8. Direct Support Testing

Upon completion of repairs within the equipment, preform all appropriate tests to verify the repair. Tests should be localized in the faulted area.

Table 3-3. Backplane Point-to-Point Wiring List Card Cage

Description	Component connection To	From	Remarks
	NOTE Same routing must be used as replaced wire.		
30 AWG WHITE	E12-4	J24-9	AC FAIL
	J18-76	J24-36	AGC RESET
	J20-56	J24-48	BC10A
	J21-56	J24-3	BC10B
	J20-62	J24-50	BC2A
	J21-62	J24-5	BC2B
	J20-23	J24-78	CLK A
	J21-23	J24-89	CLK B
	J20-66	J24-53	CLK ER A
	J21-66	J24-8	CLK ER B
30 AWG TW PR*	E10-A27	J24-62	CLOCK ERROR
30 AWG WHITE	J20-59	J21-59	CLR
	J21-59	J24-11	CLR
	J22-30	J19-20	CT DISABLE A
	J23-30	J19-64	CT DISABLE B
30 AWG TW PR*	J18-59	J17-23	DATA INPUT-1
	J17-23	J16-23	DATA INPUT-1
	J16-23	J15-23	DATA INPUT-1
	J15-23	J14-23	DATA INPUT-1
	J14-23	J13-23	DATA INPUT-1
	J13-23	J21-23	DATA INPUT-1
	J12-23	J11-23	DATA INPUT-1
	J11-23	J10-23	DATA INPUT-1
	J18-58	J17-22	DATA INPUT-2
	J17-22	J16-22	DATA INPUT-2
	J16-22	J15-22	DATA INPUT-2
	J15-22	J14-22	DATA INPUT-2
	J14-22	J13-22	DATA INPUT-2
	J13-22	J12-22	DATA INPUT-2
	J12-22	J11-22	DATA INPUT-2
	J11-22	J10-22	DATA INPUT-2
30 AWG WHITE	J26-20	J24-13	DISK A OK
	J20-64	J24-34	DISK A RDY
	J26-11	J24-14	DISK B OK
	J21-64	J24-79	DISK B RDY
	J20-57	J24-2	DISK RDY
			DISK OP
			RST A
	J21-57	J24-47	DISK RDY
			DISK OP
			RST B
	E11-2	J24-67	DISK RDY LMP A
	E11-3	J24-23	DISK RDY LMP B
	J20-53	J24-21	DISK SEL A
	J21-53	J24-65	DISK SEL B
	J20-21	J24-49	DT A
30 AWG TW PR*	J21-21	J24-4	DT B

Table 3-3. Backlane Point-to-Point Wiring List Card Cage-Continued

Description	Component connection To	From	Remarks
30 AWG TW PR*	J26-87	J24-80	EN SEL
30 AWG TW PR*	E10-A31	E24-75	ERROR RESET
20 AWG WHITE	E11-5	J10-32	GROUND
30 AWG TW PR*	E10-A25	J24-85	INDEX CLOCK +
30 AWG WHITE	E12-2	J20-47	INT LK RDY A
	E12-3	J21-47	INT LK RDY B
	E12-6	J24-55	LAMP TEST
30 AWG TW PR*	E10-49	J24-84	MASTER CLOCK
30 AWG WHITE	J20-60	J24-42	OPA
30 AWG WHITE	J21-60	J24-86	OPB
30 AWG TW PR*	E10-A29	J24-61	PARITY ERROR
30 AWG WHITE	J20-46	J21-46	PS RDY
	E12-1	J20-46	PS RDY
	J18-77	J24-22	RA CLK
	J26-5	J24-18	RAS SEL
	J24-18	J23-89	RAS SEL
	J23-89	J22-89	RAS SEL
	J18-74	J24-15	RD
	J18-75	J24-6	RD CLK
30 AWG TW PR*	E10-A41	J24-76	READ ENABLE
	E10-A1	J24-64	READ DATA
	E10-A3	J24-63	READ/WRITE CLOCK
	J24-57	J20-22	RECV OS A
	J24-58	J21-22	RECV OS B
30 AWG WHITE	J18-78	J24-66	REN
30 AWG TW PR*	J24-16	J20-20	RETURN
	J24-17	J21-20	RETURN
	E10-A2	J24-20	RETURN
	E10-A4	J24-19	RETURN
	E10-A6	J24-37	RETURN
	E10-A8	J24-38	RETURN
	E10-A10	J24-40	RETURN
	E10-A12	J21-5	RETURN
	J21-5	J20-5	RETURN
	E10-A14	J21-6	RETURN
	J21-6	J20-6	RETURN
	E10-A16	J21-3	RETURN
	J21-3	J20-3	RETURN
	E10-A18	J21-4	RETURN
	J21-4	J20-4	RETURN
	E10-A20	J21-9	RETURN
	J21-9	J20-9	RETURN
	E10-A22	J21-10	RETURN
	J21-10	J20-10	RETURN
	E10-A24	J21-7	RETURN
	J21-7	J20-7	RETURN
	E10-A26	J24-41	RETURN
	E10-A28	J24-17	RETURN
	E10-A30	J24-16	RETURN
	E10-A32	J24-31	RETURN
	E10-A40	J24-33	RETURN
	E10-A42	J24-32	RETURN
	E10-A44	J24-30	RETURN
30 AWG WHITE	J20-61	J24-44	SECT CLK A
30 AWG WHITE	J21-61	J24-88	SECT CLK B
30 AWG TW PR*	E10-A11	J21-50	SECTOR ADD LINE 0
	J21-50	J20-50	SECTOR ADD LINE 0
	E10-A13	J21-51	SECTOR ADD LINE 1
	J21-51	J20-51	SECTOR ADD LINE 1
	E10-A15	J21-48	SECTOR ADD LINE 2
	J21-48	J20-48	SECTOR ADD LINE 2
	E10-A17	J21-49	SECTOR ADD LINE 3

Table 3-3. Backlane Point-to-Point Wiring List Card Cage-Continued

Description	Component connection To	From	Remarks
30 AWG TW PR*	J21-49	J20-49	SECTOR ADD LINE 3
	E10-A19	J21-54	SECTOR ADD LINE 4
	J21-54	J20-54	SECTOR ADD LINE 4
	E10-A21	J21-55	SECTOR ADD LINE 5
	J21-55	J20-55	SECTOR ADD LINE 5
	E10-A23	J21-52	SECTOR ADD LINE 6
	J21-52	J20-52	SECTOR ADD LINE 6
	E10-A7	J24-82	SECTOR ADD STROBE
	E10-A5	J24-81	SECTOR CLOCK
30 AWG WHITE	J20-63	J24-43	SECT STRB A
	J21-63	J24-87	SECT STRB B
	E12-5	J24-12	SEQ DN
	J26-34	J23-42	TA0
	J23-42	J22-42	TA0
	J22-42	J19-17	TA0
	J26-39	J23-43	TA1
	J23-43	J22-43	TA1
	J22-43	J19-62	TA1
	J26-38	J23-44	TA2
	J23-44	J22-44	TA2
	J22-44	J19-18	TA2
	J26-37	J23-45	TA3
	J23-45	J22-45	TA3
	J22-45	J19-63	TA3
	J26-12	J23-90	TA4
	J23-90	J22-90	TA4
	J22-90	J19-19	TA4
	J26-18	J23-32	TA5
	J23-32	J22-32	TA5
	J22-33	J13-1	TA5A
	J13-1	J12-1	TA5A
	J12-1	J11-1	TA5A
	J11-1	J10-1	TA5A
	J23-33	J17-1	TA5B
	J17-1	J16-1	TA5B
	J16-1	J15-1	TA5B
	J15-1	J14-1	TA5B
	J26-16	J23-6	TA6
	J23-6	J22-6	TA6
	J22-34	J13-2	TA6A
	J13-2	J12-2	TA6A
	J12-2	J11-2	TA6A
	J11-2	J10-2	TA6A
	J23-34	J17-2	TA6B
	J17-2	J16-2	TA6B
	J16-2	J15-2	TA6B
	J15-2	J14-2	TA6B
	J26-15	J23-7	TA7
	J23-7	J22-7	TA7
	J26-86	J22-8	TA7
	J26-40	J23-8	TA7
	J26-8	J23-9	TA8
	J23-9	J22-9	TA8
	J26-42	J22-10	TA8A
	J26-41	J23-10	TA8B
	J26-7	J24-35	TA9
	J24-35	J22-17	TA9
	J26-6	J23-17	TA9
	J26-89	J10-4	TRUNK SEL 0A
	J26-4	J14-4	TRUNK SEL 0B
	J26-44	J11-4	TRUNK SEL 1A
	J26-3	J15-4	TRUNK SEL 1B

Table 3-3. Backlane Point-to-Point Wiring List Card Cage-Continued

Description	Component connection To	From	Remarks
30 AWG WHITE	J26-88	J12-4	TRUNK SEL 2A
	J26-47	J16-4	TRUNK SEL 2B
	J26-43	J13-4	TRUNK SEL 3A
	J26-2	J17-4	TRUNK SEL 3B
	E11-1	J26-19	UNIT SEL SW
	J24-60	J11-24	WCLK-1
	J11-42	J10-42	WCLK-1
	J24-59	J13-42	WCLK-2
	J13-42	J12-42	WCLK-2
	J24-56	J15-42	WCLK-3
	J15-42	J14-42	WCLK-3
	J24-10	J17-42	WCLK-4
	J17-42	J16-42	WCLK-4
	J20-58	J24-54	WC53A
	J21-58	J24-51	WC53B
	J24-83	J13-3	WEN-1
	J13-3	J12-3	WEN-1
	J12-3	J11-3	WEN-1
	J11-3	J10-3	WEN-1
	J24-39	J17-3	WEN-2
	J17-3	J16-3	WEN-2
	J16-3	J15-3	WEN-2
	J15-3	J14-3	WEN-2
	J21-65	J24-7	WRD1 B
	J10-5	J11-5	WRITE CURRENT
	J11-5	J12-5	
	J12-5	J13-5	
	J13-5	J14-5	
	J14-5	J15-5	
	J15-5	J16-5	
	J16-5	J17-5	
	J10-30	J11-30	
	J11-30	J12-30	
	J12-30	J13-30	
	J13-30	J14-30	
	J14-30	J15-30	
	J15-30	J16-30	
	J16-30	J17-30	
30 AWG TW PR*	E10-A43	J24-74	WRITE DATA LINE
30 AWG TW PR*	E10-A39	J24-77	WRITE ENABLE
30 AWG WHITE	J20-65	J24-52	WRK1 A
30 AWG WHITE	E11-4	J10-29	−12V

*TW PR = Twisted Pair

Table 3-4. Card Cage Harness Point-to-Point Wiring List (Fig. FO-2)

Description	Component connection From	To	Remarks
	NOTE Same routing must be used as replaced wire.		
26 AWG WHITE	DS1-1	E11-2	DISK RDY LMP A
	DS1-2	DS2-2	−12V
	DS2-1	E11-3	DISK RDY LMP B
	DS2-2	DS1-2	−12V
	DS2-2	E11-4	−12V
16	E1-1	J1-G	GROUND
26	E1-2	J4-HH	GROUND
	E1-3	J5-HH	GROUND
	E1-4	J6-HH	GROUND
	E1-5	J7-HH	GROUND
16	E2	J1-F	WRITE CURRENT
	E3	J1-D	+WV
	E4	J1-H	GROUND
	E5	J1-A	+5V
	E6	J1-C	+12V
	E7	J1-E	−12V
	E8	J1-J	GROUND
	E9	J1-B	+5V
26 AWG TW PR	E10-A1	J2-A	READ DATA
26 AWG TW PR	E10-A2	J2-B	RETURN
	E10-A3	J2-C	READ/WRITE CLOCK
	E10-A4	J2-D	RETURN
	E10-A5	J2-E	SECTOR CLOCK
	E10-A6	J2-F	RETURN
	E10-A7	J2-G	SECTOR ADD STROBE
	E10-A8	J2-H	RETURN
	E10-A9	J2-J	MASTER CLOCK
	E10-A10	J2-K	RETURN
	E10-A11	J2-V	SECTOR ADD LINE 0
	E10-A12	J2-W	RETURN
	E10-A13	J2-X	SECTOR ADD LINE 1
	E10-A14	J2-Y	RETURN
	E10-A15	J2-Z	SECTOR ADD LINE 2
	E10-A16	J2-a	RETURN
	E10-A17	J2-b	SECTOR ADD LINE 3
	E10-A18	J2-c	RETURN
	E10-A19	J2-d	SECTOR ADD LINE 4
	E10-A20	J2-e	RETURN
	E10-A21	J2-f	SECTOR ADD LINE 5
	E10-A22	J2-g	RETURN
	E10-A23	J2-h	SECTOR ADD LINE 6
	E10-A24	J2-i	RETURN
	E10-A25	J2-j	INDEX CLOCK
	E10-A26	J2-k	RETURN
	E10-A27	J2-m	CLOCK ERROR
	E10-A28	J2-n	RETURN
	E10-A29	J2-p	PARITY ERROR
	E10-A30	J2-q	RETURN
	E10-A31	J2-r	ERROR RESET
	E10-A32	J2-s	RETURN
	E10-A39	J3-f	WRITE ENABLE LINE
	E10-A40	J3-g	RETURN
	E10-A41	J3-h	READ ENABLE LINE
	E10-A42	J3-I	RETURN
	E10-A43	J3-j	WRITE DATA LINE
	E10-A44	J3-k	RETURN
	E10-C7	J3-M	RETURN
	E10-C8	J3-L	TRACK ADD LINE 1
	E10-C9	J3-P	RETURN

Table 3-4. Card Cage Harness Point-to-Point Wiring List (Fig. FO-2)--Continued

Description	Component connection From	To	Remarks
26 AWG TW PR	E10-C10	J3-N	TRACK ADD LINE 2
	E10-C11	J3-S	RETURN
	E10-C12	J3-R	TRACK ADD LINE 3
	E10-C13	J3-K	RETURN
	E10-C14	J3-J	TRACK ADD LINE 0
	E10-C15	J2-L	RDY DISK 1A
	E10-C16	J2-M	RETURN
	E10-C17	J2-N	RDY DISK 1B
	E10-C18	J2-P	RETURN
	E10-C25	J2-T	RDY RISK 2B
	E10-C26	J2-U	RETURN
	E10-C27	J2-R	RDY DISK 2A
	E10-C28	J2-S	RETURN
	E10-C29	J3-V	TRACK ADD LINE 5
	E10-C30	J3-W	RETURN
	E10-C31	J3-X	TRACK ADD LINE 6
	E10-C32	J3-Y	RETURN
	E10-C33	J3-Z	TRACK ADD LINE 7
	E10-C34	J3-a	RETURN
	E10-C35	J3-T	TRACK ADD LINE 4
	E10-C36	J3-U	RETURN
	E10-C37	J3-C	RAS SELECT LINE 2
	E10-C38	J3-D	RETURN
	E10-C39	J3-b	TRACK ADD LINE 8
	E10-C40	J3-c	RETURN
	E10-C41	J3-d	TRACK ADD LINE 9
	E10-C42	J3-e	RETURN
	E10-C43	J3-A	RAS SELECT LINE 1
	E10-C44	J3-B	RETURN
26 AWG BLACK	E11-1	S1-1	UNIT SEL SW
26 AWG WHITE	E11-2	DS1-1	DISK RDY LMP A
	E11-3	DS2-1	DISK RDY LMP B
	E11-4	DS2-2	−12V
26 AWG BLACK	E11-5	S1-2	GROUND
26 AWG WHITE	E12-1	J1-S	PS RDY
	E12-2	J4-CC	INT LK RDY A
	E12-2	J4-CC	INT LK RDY B
	E12-4	J1-P	AC FAIL
	E12-5	J1-R	SEQ DN
	E12-6	J1-V	LAMP TEST
	E12-7	J10-17	GROUND
	E12-8	J10-18	GROUND
16 AWG WHITE	J1-A	E5	+5V
	J1-B	E9	+5V
	J1-C	E6	+12V
	J1-D	E3	+WV
	J1-E	E7	−12V
	J1-F	E2	WRITE CURRENT
16 AWG BLACK	J1-G	E1-1	GROUND
16 AWG BLACK	J1-H	E4	GROUND
16 AWG BLACK	J1-J	E8	GROUND
16 AWG WHITE	J1-P	E12-4	AC FAIL
16 AWG WHITE	J1-R	E12-5	SEQ DN
	J1-S	E12-1	PS RDY
	J1-V	E12-6	LAMP TEST
	J1-W	J5-DD	INT LK RDY A
26 AWG WHITE	J1-X	J7-DD	INT LK RDY B
26 AWG TW PR	J2-A	E10-A1	READ DATA
	J2-B	E10-A2	RETURN
	J2-C	E10-A3	READ/WRITE CLOCK
	J2-D	E10-A4	RETURN
	J2-E	E10-A5	SECTOR CLOCK

Table 3-4. Card Cage Harness Point-to-Point Wiring List (Fig. FO-2)-Continued

Description	Component connection From	To	Remarks
26 AWG TW PR	J2-F	E10-A6	RETURN
	J2-G	E10-A7	SECTOR ADD STROBE
	J2-H	E10-A8	RETURN
	J2-J	E10-A9	MASTER CLOCK
	J2-K	E10-A10	RETURN
	J2-L	E10-C15	RDY DISK 1A
	J2-M	E10-C16	RETURN
	J2-N	E10-C17	RDY DISK 1B
	J2-P	E10-C18	RETURN
	J2-R	E10-C27	RDY DISK 2A
	J2-S	E10-C28	RETURN
	J2-T	E10-C25	RDY DISK 2B
	J2-U	E10-C26	RETURN
	J2-V	E10-A11	SECTOR ADD LINE 0
	J2-W	E10-A12	RETURN
	J2-X	E10-A13	SECTOR ADD LINE 1
	J2-Y	E10-A14	RETURN
	J2-Z	E10-A15	SECTOR ADD LINE 2
	J2-a	E10-A16	RETURN
	J2-b	E10-A17	SECTOR ADD LINE 3
	J2-c	E10-A18	RETURN
	J2-d	E10-A19	SECTOR ADD LINE 4
	J2-e	E10-A20	RETURN
	J2-f	E10-A21	SECTOR ADD LINE 5
	J2-g	E10-A22	RETURN
	J2-h	E10-A23	SECTOR ADD LINE 6
	J2-i	E10-A24	RETURN
	J2-j	E10-A25	INDEX CLOCK
	J2-k	E10-A26	RETURN
	J2-m	E10-A27	CLOCK ERROR
	J2-n	E10-A28	RETURN
	J2-p	E10-A29	PARITY ERROR
	J2-q	E10-A30	RETURN
	J2-r	E10-A31	ERROR RESET
	J2-s	E10-A32	RETURN
	J3-A	E10-C43	RAS SELECT LINE 1
	J3-B	E10-C44	RETURN
	J3-C	E10-C37	RAS SELECT LINE 2
	J3-D	E10-C38	RETURN
	J3-I	E10-A42	RETURN
	J3-J	E10-C14	TRACK ADD LINE 0
	J3-K	E10-C13	RETURN
	J3-L	E10-C8	TRACK ADD LINE 1
	J3-M	E10-C7	RETURN
	J3-N	E10-C10	TRACK ADD LINE 2
	J3-P	E10-C9	RETURN
	J3-R	E10-C12	TRACK ADD LINE 3
	J3-S	E10-C12	RETURN
	J3-T	E10-C35	TRADE ADD LINE 4
	J3-U	E10-C36	RETURN
	J3-V	E10-C29	TRACK ADD LINE 5
	J3-W	E10-C30	RETURN
	J3-X	E10-C31	TRACK ADD LINE 6
	J3-Y	E10-C32	RETURN
	J3-Z	E10-C33	TRACK ADD LINE 7
	J3-a	E10-C34	RETURN
	J3-b	E10-C39	TRACK ADD LINE 8
	J3-c	E10-C40	RETURN
	J3-d	E10-C41	TRACK ADD LINE 9
	J3-e	E10-C42	RETURN
	J3-f	E10-A39	WRITE ENABLE LINE
	J3-g	E10-A40	RETURN

Table 3-4. Card Cage Harness Point-to-Point Wiring List (Fig. FO-2)-Continued

Description	Component connection From	To	Remarks
26 AWG TW PR	J3-h	E10-A41	READ ENABLE LINE
	J3-j	E10-A43	WRITE DATA LINE
	J3-k	E10-A44	RETURN
26 AWG SH TW PR*	J4-A	J10-37	TRUNK 0
	J4-B	J11-37	TRUNK 4
	J4-C	J10-35	TRUNK 1
	J4-D	J11-35	TRUNK 5
	J4-E	J10-13	TRUNK 2
	J4-F	J11-13	TRUNK 6
	J4-G	J10-11	TRUNK 3
	J4-H	J11-11	TRUNK 7
26 AWG WHITE	J4-J	J19-90	CT00A
	J4-K	J19-89	CT01A
	J4-L	J19-88	CT02A
	J4-M	J19-87	CT03A
	J4-N	J19-86	CT04A
	J4-P	J19-85	CT05A
	J4-R	J19-84	CT06A
	J4-S	J19-83	CT07A
	J4-T	J19-82	CT08A
	J4-U	J19-81	CT09A
26 AWG SH TW PR*	J4-V	J10-38	TRUNK 0
		J10-G	SHIELD
	J4-W	J11-38	TRUNK 4
		J11-G	SHIELD
	J4-X	J10-36	TRUNK 1
		J10-G	SHIELD
	J4-Y	J11-36	TRUNK 5
		J11-G	SHIELD
	J4-Z	J10-14	TRUNK 2
		J10-G	SHIELD
26 AWG WHITE	J4-AA	J19-48	CT29A
	J4-BB	J19-47	CT30A
	J4-CC	E12-2	INT LK RDY A
	J4-DD	J5-CC	INT LK RDY A
	J4-EE	J19-46	CT31A
	J4-FF	J22-18	SCT0A
	J4-GG	J22-4	SCT1A
	J4-HH	E1-2	GROUND
26 AWG SH TW PR*	J4-a	J11-14	TRUNK 6
		J11-G	SHIELD
	J4-b	J10-12	TRUNK 3
		J10-G	SHIELD
	J4-C	J11-12	TRUNK 7
		J11-G	SHIELD
26 AWG WHITE	J4-f	J19-80	CT10A
	J4-g	J19-79	CT11A
	J4-h	J19-78	CT12A
	J4-i	J19-77	CT13A
	J4-j	J19-76	CT14A
	J4-k	J19-75	CT15A
	J4-m	J19-61	CT16A
	J4-n	J19-60	CT17A
	J4-p	J19-59	CT18A
	J4-q	J19-58	CT19A
	J4-r	J19-57	CT20A
	J4-s	J19-56	CT21A
	J4-t	J19-55	CT22A
	J4-u	J19-54	CT23A
	J4-v	J19-53	CT24A
	J4-w	J19-52	CT25A
	J4-x	J19-51	CT26A

Table 3-4. Card Cage Harness Point-to-Point Wiring List (Fig. FO-2)-Continued

Description	Component connection From	To	Remarks
26 AWG WHITE	J4-y	J19-50	CT27A
	J4-z	J19-49	CT28A
26 AWG SH TW PR*	J‡-A	J12-37	TRUNK 8
	J5-B	J13-37	TRUNK 12
	J5-C	J12-35	TRUNK 9
	J5-D	J13-35	TRUNK 13
	J5-E	J12-13	TRUNK 10
	J5-F	J13-13	TRUNK 14
	J5-G	J12-11	TRUNK 11
	J5-H	J13-11	TRUNK 15
	J5-J	J19-90	CT00A
26 AWG WHITE	J5-K	J19-89	CT01A
	J5-L	J19-88	CT02A
	J5-M	J19-87	CT03A
	J5-N	J19-86	CT04A
	J5-P	J19-85	CT05A
	J5-R	J19-84	CT06A
	J5-S	J19-83	CT07A
	J5-T	J19-82	CT08A
	J5-U	J19-81	CT09A
26 AWG SH TW PR*	J5-V	J12-38	TRUNK 8
		J12-G	SHIELD
	J5-W	J13-38	TRUNK 12
		J13-G	SHIELD
	J5-X	J12-36	TRUNK 9
		J12-G	SHIELD
	J5-Y	J13-36	TRUNK 13
		J13-G	SHIELD
	J5-Z	J12-14	TRUNK 10
		J12-G	SHIELD
26 AWG WHITE	J5-AA	J19-48	CT29A
	J5-BB	J19-47	CT30A
	J5-CC	J4-DD	INT LK RDY A
	J5-DD	J1-W	INT LK RDY A
	J5-EE	J19-46	CT31A
	J5-FF	J22-18	SCT0A
	J5-GG	J22-4	SCT1A
	J5-HH	E1-3	GROUND
26 AWG SH TW PR*	J5-a	J13-14	TRUNK 14
		J13-G	SHIELD
	J5-b	J12-12	TRUNK 11
		J12-G	SHIELD
	J5-c	J13-12	TRUNK 15
		J13-G	SHIELD
26 AWG WHITE	J5-f	J19-80	CT10A
	J5-g	J19-79	CT11A
	J5-h	J19-78	CT12A
	J5-i	J19-77	CT13A
	J5-j	J19-76	CT14A
	J5-k	J19-75	CT15A
	J5-m	J19-61	CT16A
	J5-n	J19-60	CT17A
	J5-p	J19-59	CT18A
	J5-q	J19-58	CT19A
	J5-r	J19-57	CT20A
	J5-s	J19-56	CT21A
	J5-t	J19-55	CT22A
	J5-u	J19-54	CT23A
	J5-v	J19-53	CT24A
	J5-w	J19-52	CT25A
	J5-x	J19-51	CT26A
	J5-y	J19-50	CT27A
	J5-z	J19-49	CT28A

Table 3-4. Card Cage Harness Point-to-Point Wiring List (Fig. FO-2)-Continued

Description	Component connection From	To	Remarks
26 AWG SH TW PR*	J6-A	J14-37	TRUNK 16
	J6-B	J15-37	TRUNK 20
	J6-C	J14-35	TRUNK 17
	J6-D	J15-35	TRUNK 21
	J6-E	J14-13	TRUNK 18
	J6-F	J15-13	TRUNK 22
	J6-G	J14-11	TRUNK 19
	J6-H	J15-11	TRUNK 23
26 AWG WHITE	J6-J	J19-45	CT00B
	J6-K	J19-44	CT01B
	J6-L	J19-43	CT02B
	J6-M	J19-42	CT03B
	J6-N	J19-41	CT04B
	J6-P	J19-40	CT05B
	J6-R	J19-39	CT06B
	J6-S	J19-38	CT07B
	J6-T	J19-37	CT08B
	J6-U	J19-36	CT09B
26 AWG SH TW PR*	J6-V	J14-38	TRUNK 16
		J14-G	SHIELD
	J6-W	J15-38	TRUNK 20
		J15-G	SHIELD
	J6-X	J14-36	TRUNK 17
		J14-G	SHIELD
	J6-Y	J15-36	TRUNK 21
		J15-G	SHIELD
	J6-Z	J14-14	TRUNK 18
		J14-G	SHIELD
26 AWG WHITE	J6-AA	J19-3	CT29B
	J6-BB	J19-2	CT30B
	J6-CC	E12-3	$\overline{\text{INT LK RDY B}}$
	J6-DD	J7-CC	$\overline{\text{INT LK RDY B}}$
	J6-EE	J19-1	CT31B
	J6-FF	J23-18	SCT0B
	J6-GG	J23-4	SCT1B
	J6-HH	E1-4	GROUND
26 AWG SH TW PR*	J6-2	J15-14	TRUNK 22
		J15-G	SHIELD
	J6-b	J14-12	TRUNK 19
		J14-G	SHIELD
	J6-c	J15-12	TRUNK 23
		J15-G	SHIELD
26 AWG WHITE	J6-f	J19-35	CT10B
	J6-g	J19-34	CT11B
	J6-h	J19-33	CT12B
	J6-i	J19-32	CT13B
	J6-j	J19-31	CT14B
	J6-k	J19-30	CT15B
	J6-m	J19-16	CT16B
	J6-n	J19-15	CT17B
	J6-p	J19-14	CT18B
	J6-q	J19-13	CT19B
	J6-r	J19-12	CT20B
	J6-s	J19-11	CT21B
	J6-t	J19-10	CT22B
	J6-u	J19-9	CT23B
	J6-v	J19-8	CT24B
	J6-w	J19-7	CT25B
	J6-x	J19-6	CT26B
	J6-y	J19-5	CT27B
	J6-z	J19-4	CT28B

Table 3-4. Card Case Harness Point-to-Point Wiring List (Fig. FO-2)--Continued

Description	Component connection From	To	Remarks
26 AWG SH TW PR*	J7-A	J16-37	TRUNK 24
	J7-B	J17-37	TRUNK 28
	J7-C	J16-35	TRUNK 25
	J7-D	J17-35	TRUNK 29
	J7-E	J16-13	TRUNK 26
	J7-F	J17-13	TRUNK 30
	J7-G	J16-11	TRUNK 27
	J7-H	J17-11	TRUNK 31
26 AWG WHITE	J7-J	J19-45	CT00B
	J7-K	J19-44	CT01B
	J7-L	J19-43	CT02B
	J7-M	J19-42	CT03B
	J7-N	J19-41	CT04B
	J7-P	J19-40	CT05B
	J7-R	J19-39	CT06B
	J7-S	J19-38	CT07B
	J7-T	J19-37	CT08B
	J7-U	J19-36	CT09B
26 AWG SH TW PR*	J7-V	J16-38	TRUNK 24
		J16-G	SHIELD
	J7-W	J17-38	TRUNK 28
		J17-G	SHIELD
	J7-X	J16-36	TRUNK 25
		J16-G	SHIELD
	J7-Y	J17-36	TRUNK 29
		J17-G	SHIELD
	J7-Z	J16-14	TRUNK 26
		J16-G	SHIELD
26 AWG WHITE	J7-AA	J19-3	CT29B
	J7-BB	J19-2	CT30B
	J7-CC	J6-DD	$\overline{\text{INT LK RDY B}}$
	J7-DD	J1-X	INT LK RDY B
	J7-EE	J19-1	CT31B
	J7-FF	J23-18	SCT0B
	J7-GG	J23-4	SCT1B
	J7-HH	E1-5	GROUND
26 AWG SH TW PR*	J7-a	J17-14	TRUNK 30
		J17-G	SHIELD
	J7-b	J16-12	TRUNK 27
		J16-G	SHIELD
	J7-c	J17-12	TRUNK 31
		J17-G	SHIELD
	J7-f	J19-35	CT10B
	J7-g	J19-34	CT11B
	J7-h	J19-33	CT12B
	J7-i	J19-32	CT13B
	J7-j	J19-31	CT14B
	J7-k	J19-30	CT15B
	J7-m	J19-16	CT16B
	J7-n	J19-15	CT17B
	J7-p	J19-14	CT18B
	J7-q	J19-13	CT19B
	J7-r	J19-12	CT20B
	J7-s	J19-11	CT21B
	J7-t	J19-10	CT22B
	J7-u	J19-9	CT23B
	J7-v	J19-8	CT24B
	J7-w	J19-7	CT25B
	J7-x	J19-6	CT26B
	J7-y	J19-5	CT27B
	J7-z	J19-4	CT28B
26 AWG SH TW PR*	J8-A	J20-89	CLOCK HD 1A

Table 3-4. Card Cage Harness Point-to-Point Wiring List (Fig. FO-2)-Continued

Description	Component connection From	To	Remarks
26 AWG WHITE	J8-B	J20-86	CLOCK HD A CT
26 AWG SH TW PR*	J8-C	J20-90	
		J20-G	SHIELD
	J8-D	J20-88	CLOCK HD 2A
	J8-F	J20-87	
		J20-G	SHIELD
	J9-A	J21-89	CLOCK HD 1B
26 AWG SH WHITE	J9-B	J21-86	CLOCK HD B CT
26 AWG SH TW PR*	J9-C	J21-90	
		J21-G	SHIELD
	J9-D	J21-88	CLOCK HD 2B
	J9-F	J21-87	
		J21-G	SHIELD
	J10-11	J4-G	TRUNK 3
	J10-12	J4-b	TRUNK 3
	J10-13	J4-E	TRUNK 2
	J10-14	J4-Z	TRUNK 2
	J10-17	E12-7	GROUND
	J10-18	E12-8	GROUND
	J10-35	J4-C	TRUNK 1
	J10-36	J4-X	TRUNK 1
	J10-37	J4-A	TRUNK 0
	J10-38	J4-V	TRUNK 0
	J11-11	J4-H	TRUNK7
	J11-12	J4-c	TRUNK 7
	J11-13	J4-F	TRUNK 6
	J11-14	j4-a	TRUNK 6
	J11-35	J4-D	TRUNK 5
	J11-36	J4-Y	TRUNK 5
	J11-37	J4-B	TRUNK 4
	J11-38	J4-W	TRUNK 4
	J12-11	J5-G	TRUNK 11
	J12-12	J5-b	TRUNK 11
	J12-13	J5-E	TRUNK 10
	J12-14	J5-Z	TRUNK 10
	J12-35	J5-C	TRUNK 9
	J12-36	J5-X	TRUNK 9
	J12-37	J5-A	TRUNK 8
	J12-38	J5-V	TRUNK 8
	J13-11	J5-H	TRUNK 15
	J13-12	J5-c	TRUNK 15
	J13-13	J5-F	TRUNK 14
	J13-14	J5-a	TRUNK 14
	J13-35	J5-D	TRUNK 13
	J13-36	J5-Y	TRUNK 13
	J13-37	J5-B	TRUNK 12
	J13-38	J5-W	TRUNK 12
	J14-11	J6-G	TRUNK 19
	J14-12	J6-b	TRUNK 19
	J14-13	J6-E	TRUNK 18
	J14-14	J6-Z	TRUNK 18
	J14-35	J6-C	TRUNK 17
	J14-36	J6-X	TRUNK 17
	J14-37	J6-A	TRUNK 16
	J14-38	J6-V	TRUNK 16
	J15-11	J6-H	TRUNK 23
	J15-12	J6-c	TRUNK 23
	J15-13	J6-F	TRUNK 22
	J15-14	J6-a	TRUNK 22
	J15-35	J6-D	TRUNK 21
	J15-36	J6-Y	TRUNK 21
	J15-37	J6-B	TRUNK 20

Table 3-4. Card Cage Harness Point-to-Point Wiring List (Fig. FO-2)-Continued

Description	Component connection From	To	Remarks
26 AWG SH TW PR*	J15-38	J6-W	TRUNK 20
	J16-11	J7-C	TRUNK 27
	J16-12	J7-b	TRUNK 27
	J16-13	J7-E	TRUNK 26
	J16-14	J7-Z	TRUNK 26
	J16-35	J7-C	TRUNK 25
	J16-36	J7-X	TRUNK 25
	J16-37	J7-A	TRUNK 24
	J16-38	J7-V	TRUNK 24
	J17-11	J7-H	TRUNK 31
	J17-12	J7-c	TRUNK 31
	J17-13	J7-F	TRUNK 30
	J17-14	J7-a	TRUNK 30
	J17-35	J7-D	TRUNK 29
	J17-36	J7-Y	TRUNK 29
	J17-37	J7-B	TRUNK 28
	J17-38	J7-W	TRUNK 28
26 AWG WHITE	J19-1	J6-EE	CT31B
		J7-EE	CT31B
	J19-2	J6-BB	CT30B
		J7-BB	CT30B
	J19-3	J6-AA	CT29B
		J7-AA	CT29B
	J19-4	J6-z	CT28B
		J7-z	CT28B
	J19-5	J6-y	CT27B
		J7-y	CT27B
	J19-6	J6-x	CT26B
		J7-x	CT26B
	J19-7	J6-w	CT25B
		J7-w	CT25B
	J19-8	J6-v	CT24B
		J7-v	CT24B
	J19-9	J6-u	CT23B
		J7-u	CT23B
	J19-10	J6-t	CT22B
		J7-t	CT22B
	J19-11	J6-s	CT21B
		J7-s	CT21B
	J19-12	J6-r	CT20B
		J7-r	CT20B
	J19-13	J6-q	CT19B
		J7-q	CT19B
	J19-14	J6-p	CT18B
		J7-p	CT18B
	J19-15	J6-n	CT17B
		J7-n	CT17B
	J19-16	J6-m	CT16B
		J7-m	CT16B
	J19-30	J6-k	CT15B
		J7-k	CT15B
	J19-31	J6-j	CT14B
		J7-j	CT14B
	J19-32	J6-i	CT13B
		J7-i	CT13B
	J19-33	J6-h	CT12B
		J7-h	CT12B
	J19-34	J6-g	CT11B
		J7-g	CT11B
	J19-35	J6-f	CT10B
		J7-f	CT10B
	J19-36	J6-U	CT09B
		J7-U	CT09B

Table 3-4. Card Cage Harness Point-to-Point Wiring List (Fig. FO-2)-Continued

Description	Component connection From	To	Remarks
26 AWG WHITE	J19-37	J6-7	CT08B
		J7-T	CT08B
	J19-38	J6-S	CT07B
		J7-S	CT07B
	J19-39	J6-R	CT06B
		J7-R	CT06B
	J19-40	J6-P	CT05B
		J7-P	CT05B
	J19-41	J6-N	CT04B
		J7-N	CT04B
	J19-42	J6-M	CT03B
		J7-M	CT03B
	J19-43	J6-L	CT02B
		J7-L	CT02B
	J19-44	J6-K	CT01B
		J7-K	CT01B
	J19-45	J6-J	CT00B
		J7-J	CT00B
	J19-46	J4-EE	CT31A
		J5-EE	CT31A
	J19-47	J4-BB	CT30A
		J5-BB	CT30A
	J19-48	J4-AA	CT29A
		J5-AA	CT29A
	J19-49	J4-z	CT28A
		J5-z	CT28A
	J19-50	J4-y	CT27A
		J5-y	CT27A
	J19-51	J4-x	CT26A
		J5-x	CT26A
	J19-52	J4-w	CT25A
		J5-w	CT25A
	J19-53	J4-v	CT24A
		J5-v	CT24A
	J19-54	J4-u	CT23A
		J5-u	CT23A
	J19-55	J4-t	CT22A
		J5-t	CT22A
	J19-56	J4-s	CT21A
		J5-s	CT21A
	J19-57	J4-r	CT20A
		J5-r	CT20A
	J19-58	J4-q	CT19A
		J5-q	CT19A
	J19-59	J4-p	CT18A
		J5-p	CT18A
	J19-60	J4-n	CT17A
		J5-n	CT17A
	J19-61	J4-m	CT16A
		J5-m	CT16A
	J19-75	J4-k	CT15A
		J5-k	CT15A
	J19-76	J4-j	CT14A
		J5-j	CT14A
	J19-77	J4-i	CT13A
		J5-i	CT13A
	J19-78	J4-h	CT12A
		J5-h	CT12A
	J19-79	J4-g	CT11A
		J5-g	CT11A
	J19-80	J4-f	CT10A
		J5-f	CT10A

Table 3-4. Card Cage Harness Point-to-Point Wiring List (Fig. FO-2)-Continued

Description	Component From	connection To	Remarks
26 AWG WHITE	J19-81	J4-U	CT09A
		J5-U	CT09A
	J19-82	J4-T	CT08A
		J5-T	CT08A
	J19-83	J4-S	CT07A
		J5-S	CT07A
	J19-84	J4-R	CT06A
		J5-R	CT06A
	J19-85	J4-P	CT05A
		J5-P	CT05A
	J19-86	J4-N	CT04A
		J5-N	CT04A
	J19-87	J4-M	CT03A
		J5-M	CT03A
	J19-88	J4-L	CT02A
		J5-L	CT02A
	J19-89	J4-K	CT01A
		J5-K	CT01A
	J19-90	J4-J	CT00A
		J5-J	CT00A
	J20-86	J8-B	CLOCK HD A CT
26 AWG SH TW PR*	J20-87	J8-F	
	J20-88	J8-D	CLOCK HD 2A
	J20-89	J8-A	CLOCK HD 1A
	J20-90	J8-C	
26 AWG SH WHITE*	J21-86	J9-B	CLOCK HD B CT
26 AWG SH TW PR*	J21-87	J9-F	
	J21-88	J9-D	CLOCK HD 2B
	J21-89	J9-A	CLOCK HD 1B
	J21-90	J9-C	
26 AWG WHITE	J22-4	J4-GG	SCT1A
		J5-GG	SCT1A
	J22-18	J4-FF	SCT0A
		J5-FF	SCT0A
	J23-4	J6-GG	SCT1B
		J7-GG	SCT1B
	J23-18	J6-FF	SCT0B
		J7-FF	SCT0B
	S1-1	E11-1	UNIT SEL SW
26 AWG BLACK	S1-2	E11-5	GROUND

*SH TW PR = Shielded Twisted Pair

Table 3-5. Harness Assembly, Disc Matrix Interconnect (Fig. FO-6)

Wire Chart

Cable no.	Wire no.	J1 from	A1	A2	A3	A4	J1	Color
1	1	A	E21	-	-	-	-	White
	2	V	E22	-	-	-	-	Black
	3	C	E19	-	-	-	-	White
2	4	X	E20	-	-	-	-	Black
	5	E	-	E21	-	-	-	White
3	6	Z	-	E22	-	-	-	Black
	7	G	-	E19	-	-	-	White
4	8	b	-	E10	-	-	-	Black
	9	B	-	-	E21	-	-	White
5	10	W	-	-	E22	-	-	Black
	11	D	-	-	E19	-	-	White
6	12	Y	-	-	E20	-	-	Black
	13	F	-	-	-	E21	-	White
7	14	a	-	-	-	E22	-	Black
	15	H	-	-	-	E19	-	White
8	16	c	-	-	-	E20	-	Black
	17	J	E6	E6	E6	E6	-	White
	18	K	E2	E2	E2	E2	-	White
	19	L	E7	E7	E7	E7	-	White
	20	M	E3	E3	E3	E3	-	White
	21	N	E8	E8	E8	E8	-	White
	22	P	E4	E4	E4	E4	-	White
	23	R	E9	E9	E9	E9	-	White
	24	S	E5	E5	E5	E5	-	White
	25	T	E28	E28	E2	E28	-	White
	26	U	E36	E36	E36	E36	-	White
	27	f	E29	E29	E29	E29	-	White
	28	g	E37	E37	E37	E37	-	White
	29	h	E30	E30	E30	E30	-	White
	30	i	E38	E38	E38	E38	-	White
	31	j	E31	E31	E31	E31	-	White
	32	k	E39	E39	E39	E39	-	White
	33	m	E14	E14	E14	E14	-	White
	34	n	E10	E10	E10	E10	-	White
	35	p	E15	E15	E15	E16	-	White
	36	q	E11	E11	E11	E11	-	White
	37	r	E16	E16	E16	E16	-	White
	38	s	E12	E12	E12	E12	-	White
	39	t	E17	E17	E17	E17	-	White
	40	u	E13	E13	E13	E13	-	White
	41	v	E24	E24	E24	E24	-	White
	42	w	E32	E32	E32	E32	-	White
	43	x	E25	E25	E25	E25	-	White
	44	y	E33	E33	E33	E33	-	White
	45	z	E26	E26	E26	E26	-	White
	46	AA	E34	E34	E34	E34	-	White
	47	BB	E27	E27	E27	E27	-	White
	48	EE	E35	E35	E36	E35	-	White
	49	FF	E1	E1	E1	E1	-	White
	50	GG	E23	E23	E23	E23	-	White
	51	HH	E40	E40	E40	E40	-	White
	52	CC	-	-	-	-	DD	White
	53	A4-E40	E41					White

NOTE

Wiring for 256 track shown, each 512 track disc assembly contains two such matrices (J1 and J20.

Section IV. MAINTENANCE

3-9. General

This section provides step-by-step instructions on selecting a spare track, and removal and replacement instructions for the card cage and front panel assemblies.

NOTE

Be sure that serial number on spare Track Card agrees with serial number on spare track label of spindle assembly (fig. 3-3).

3-10. Spare Track Selection Matrix

An erroring track can be switched to a spare track through the use of the proper Spare Track Select Logic (A or B) card. This logic card, when properly jump-wired will inhibit the read/write head of the erroring track and enable a spare read/write head. It is not necessary to unsolder any wire to disable the read/write head of the erroring track. A maximum of 32 spare read/write heads are available per logic card, some of which may have been used during manufacturing. The spare track label located on the disc spindle assembly will indicate the number of tracks that have been spared for that particular disc spindle assembly. The matrix board, to which the jump-wiring is done, is mounted "piggy-back" to the component side of the logic card. This matrix board has a 32 x 32 matrix (Matrix A) and a 16 x 16 matrix (Matrix B) and is removed from the logic card during sparing to facilitate soldering (para 3-13). The matrix board, if damaged, is replaced with a new matrix board jump-wired to the same configuration as the existing board.

3-11. Octal Address

The track addresss for TAO through TA9 is converted into four digit octal address (fig. 3-2). TA9 (0) addresses disc drive A and TA9 high (1) addresses disc drive B. For further discussion, assume that the disc drive is erroring on octal address 0333. It is immediately known that the error is in disc drive-A. Octal address 333 is located in block A15(A). A15 indicates the head assembly. (A) is the row where the head core is found and the last digit of the octal address "3" indicates the column. At the left side of the table is listed the Matrix A inputs (O through 31). Since octal address 330 is input 8, octal address 333 must be input 11. At the top of the table is listed the Matrix B inputs (O through 15). Observe that octal addresses 300 through 337 are input 6. Therefore, octal address 333 is translated to: head assembly A15, core 9; Matrix A input 11; Matrix B input 6 of disc drive A. Table 3-6 illustrates how five different octal addresses are deciphered.

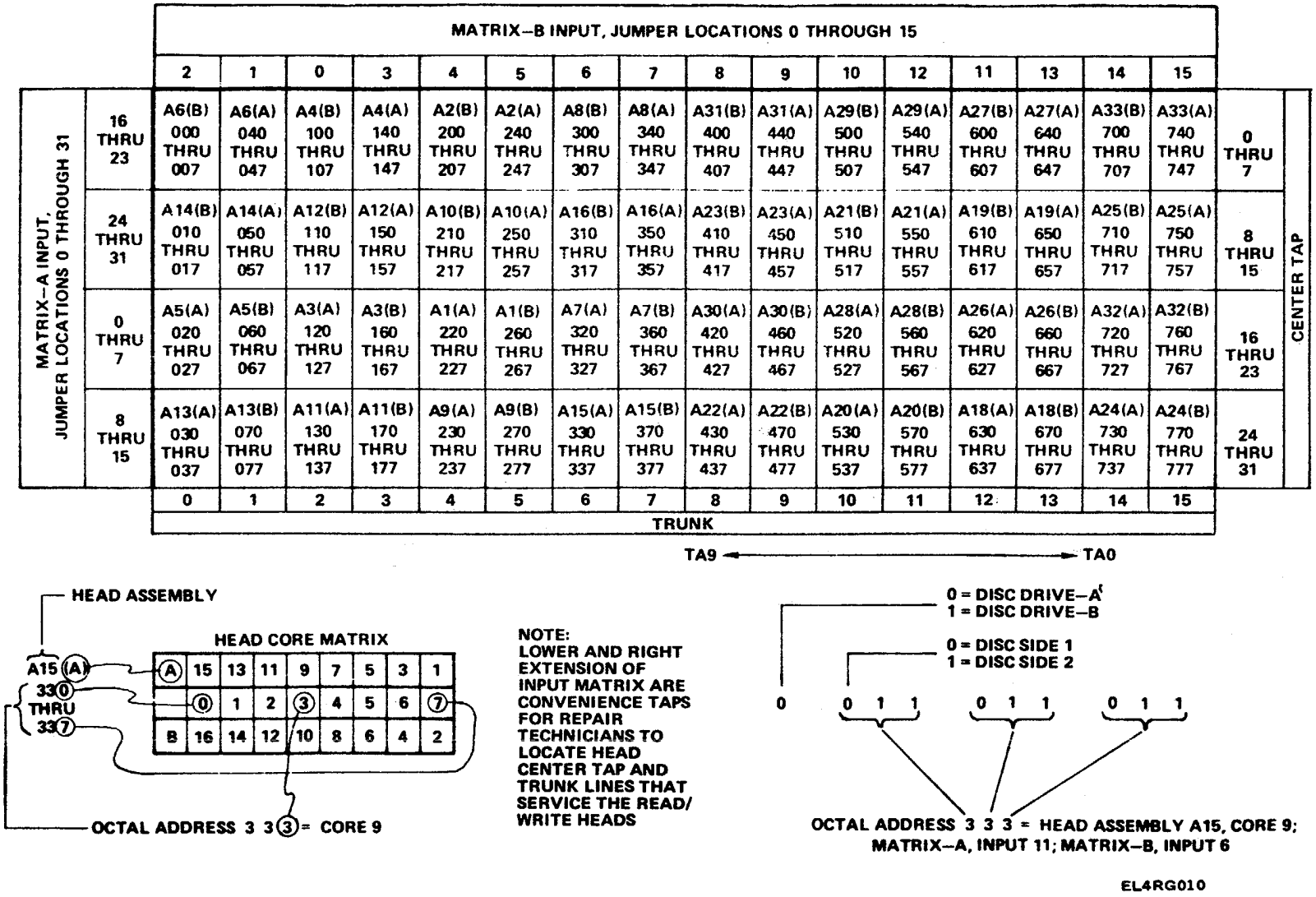


Figure 3-2. Octal Address Conversion

Table 3-6. Octal Addresses Deciphered

Octal address	Disc drive	Head Assy and core	Matrix A input	Matrix B input
1711	B	A25-14	25	14
0605	A	A27-6	21	11
1524	B	A28-7	4	10
0326	A	A7-3	6	6
0032	A	A13-11	10	2

3-12. Repair

The following are procedures in sparing erroring tracks.

a. Spare Octal Address 0333. Write down the necessary information for octal address 0333 as in the examples shown in table 3-4 (0333 A A15-9 11 6). For octal address 0333, we have a Matrix B input 6. Looking at the Spare Track Label on disc drive A (fig. 3-3), see whether a Matrix B input 6 was used previously. By inspection, we observe that it was used on spare track S5, therefore, it is advisable to spare its associate spare track S21. Referring to figure FO-5, observe that ***S21*** (gate U14B) inputs ***S21A*** and ***S5B*** are connected to MATRIX-A OUT 17 and MATRIX-B OUT 9 respectively. Spare-***S21*** as follows:

SPARE TRACKS

SPARE TRACK	IN USE OCTAL ADRS	MATRIX JUMPER LOCATIONS A	MATRIX JUMPER LOCATIONS B	UNUSABLE HEAD ASSY & CORE	SPARE TRACK	IN USE OCTAL ADRS	MATRIX JUMPER LOCATIONS A	MATRIX JUMPER LOCATIONS B	UNUSABLE HEAD ASSY & CORE
0 $\overline{S0}$	030	8	2	A13–11	16 $\overline{S16}$	020	0	2	A15–11
1 $\overline{S1}$	067	7	1	A5–2	17 $\overline{S17}$				
2 $\overline{S2}$	100	16	0	A4–16	18 $\overline{S18}$				
3 $\overline{S3}$	550	24	12	A21–15	19 $\overline{S19}$	562	2	12	A28–12
4 $\overline{S4}$	210	24	4	A10–16	20 $\overline{S20}$	236	14	4	A9–3
5 $\overline{S5}$	326	6	6	A7–3	21 $\overline{S21}$	333	11	6	A15–9
6 $\overline{S6}$	355	29	7	A16–5	22 $\overline{S22}$				
7 $\overline{S7}$	543	19	12	A29–9	23 $\overline{S23}$	576	14	12	A20–4
8 $\overline{S8}$	605	21	11	A27–6	24 $\overline{S24}$				
9 $\overline{S9}$					25 $\overline{S25}$				
10 $\overline{S10}$					26 $\overline{S26}$				
11 $\overline{S11}$					27 $\overline{S27}$				
12 $\overline{S12}$					28 $\overline{S28}$				
13 $\overline{S13}$					29 $\overline{S29}$				
14 $\overline{S14}$					30 $\overline{S30}$				
15 $\overline{S15}$					31 $\overline{S31}$				

SPINDLE ASSEMBLY SERIAL NUMBER _____

SPARE TRACK MATRIX PART NUMBER SM-D-837326- _____

EL4RG011

Figure 3-3. Spare Track Label

(1) On Matrix A, locate input 11 by output 17 as shown in figure 3-4.

(2) Insert bare wire at location and solder wire to both sides of board.

(3) Snip wire as close to board as possible.

(4) On Matrix B, locate input 6 by output 9. Observe that the location is already wired from the previous sparing of ***S5***.

(5) Scribe necessary information onto Spare Track Label as shown in figure 3-3.

b. Spare Octal Address 0605. Write down the necessary information for octal address 0605 as shown in table 3-6, (0605 A A27-6 21 11). Looking at Spare Track Label on disc drive A (fig. 3-3), no Matrix B Input 11 exists, therefore select the next spare listed which is***S8***. Referring to figure FO-4, observe that-inputs ***S8A*** and ***8B*** are connected to MATRIX-A OUT 15 and MATRIX-B OUT 7, respectively. Spare ***S8*** as follows:

(1) On Matrix A, locate input 21 by output 15 as shown in figure 3-4.

(2) Insert bare wire at location and solder wire to both sides of board.

(3) Snip wire as close to board as possible.

(4) On Matrix B, locate input 11 by output 7 as shown in figure 3-4.

(5) Insert bare wire at location and solder wire to both sides of board.

(6) Snip wire as close to board as possible.

(7) Scribe necessary information onto Spare Track. Label as shown in figure 3-3.

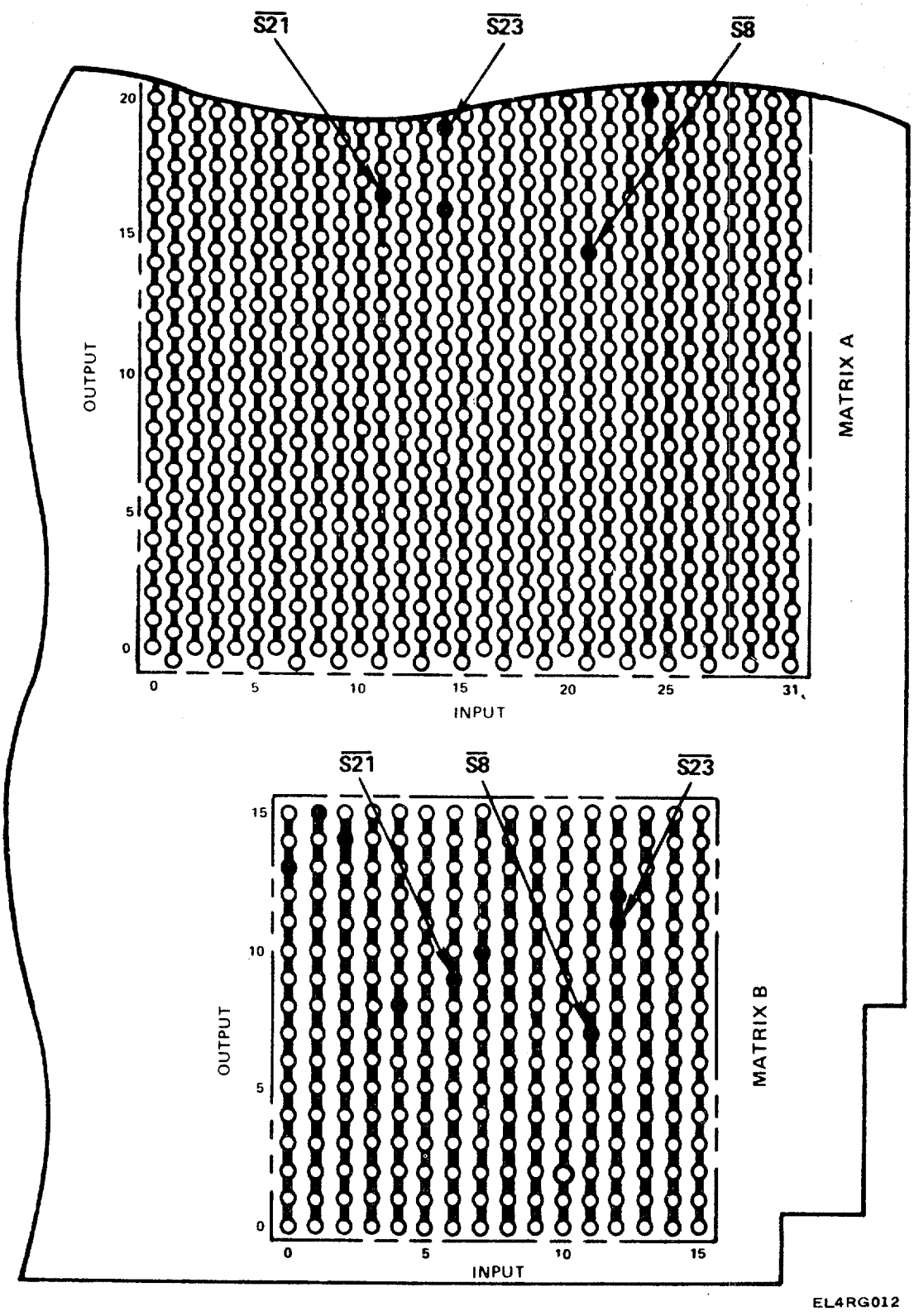


Figure 3-4. Spare Track Selection.

c. Spare Octal Address 0576. Write down the necessary information for octal address 0576 as in the examples shown in table 3-6 (0576 A A20-4 14 12). For octal address 0576 is a Matrix B Input 12 (spare S7) whose associated spare ***S23*** have not been spared. Therefore, it is advisable to spare ***S23***. Referring to figure FO-4, observe that S23 (gate 129) inputs ***S23A*** and ***S7B*** are connected to MATRIX-A OUT 19 and MATRIX-B OUT 11, respectively. Spare ***S23*** as follows:

(1) On Matrix A, locate input 14 by output 19 as shown in figure 3-4.

(2) Insert bare wire at location and solder wire to both sides of board.

(3) Snip wires as close to board as possible.

(4) On Matrix B, locate input 12 by output 11. Observe that the location is already wired from previous sparing of ***S7***.

(5) Scribe necessary information onto Spare Track Label as shown in figure 3-3.

3-13. Card Cage Assembly

NOTE

Do not make potentiometer adjustments. Refer to organizational manual TM 11-5805-683-12-1 for proper procedure.

a. Removal. Remove card cage assembly as follows (fig. 3-5):

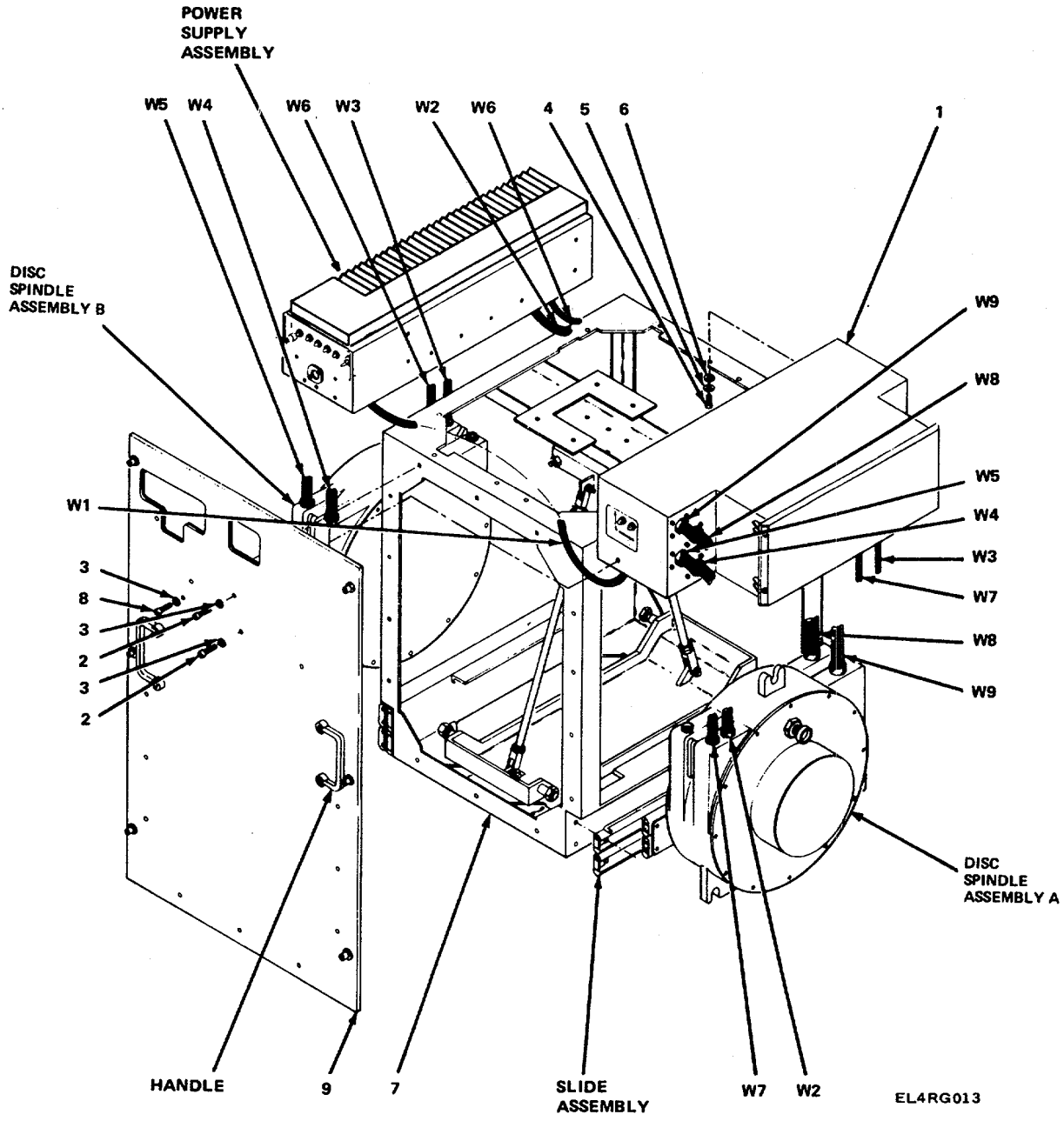


Figure 3-5. Random Access Storage Unit

(1) Disconnect following cables from card cage assembly (1, fig. 3-5). See figure 3-8 for complete cable identification.

Cable	*Card Cage Connector*
W1	J1
W3	J9
W4	J7
W5	J6
W7	J8
W8	J5
W9	J4

(2) Tag and disconnect data interface cables from connectors J2 and J3 (fig. 3-6).

(3) Remove and retain one screw (2, fig. 3-5) and washer (3, fig. 3-5) below unit ADRS switch, securing card cage to front panel assembly.

(4) Remove and retain eight screws (4), lockwashers (5), and washers (6) securing card cage to frame assembly (7, fig. 3-5).

(5) Remove card cage assembly.

CAUTION

Place card cage assembly in suitable position in work area to prevent damage to protruding connectors.

(6) Remove and retain twelve screws securing back cover to card cage.

(7) Remove back cover.

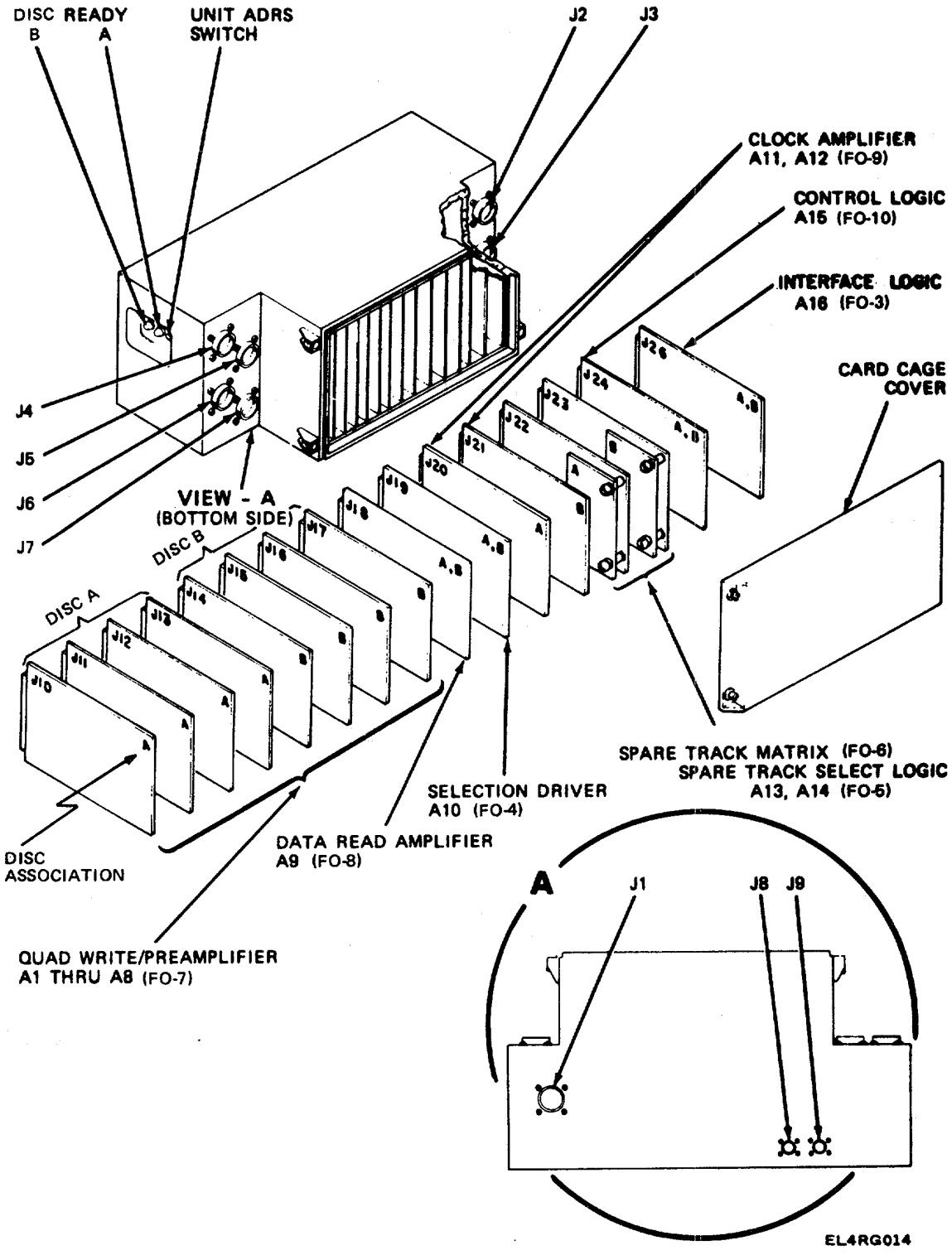


Figure 3-6. Card Cage Assembly.

b. Replacement. Install replacement or repaired card cage assembly in reverse sequence of removal instructions as follows:

(1) Install back cover using twelve screws removed in step a(6).

(2) Install card cage assembly to frame with the eight hex head screws removed in steps a(3) and a(4). Torque screws (4, fig. 3-5) to 30-inch pounds.

(3) Connect cables to card cage removed in steps a(1) and a(2).

NOTE

Refer to the Operator and Organizational Manual TM 11-5805-683-12-1, Section II, for procedures on removing disc spindle assembly A and B, and power supply assembly.

3-14. Spare Track Matrix

Each circuit card location in the card cage has upper and lower locking tabs on the card cage rail. To free the circuit card for extraction, these tabs must be extended outward until parallel with the card cage rail. Each circuit has upper and lower tabs which, when extended outward, break the card from its edge connector. The card is then free to slide out. Before reinserting circuit card, place upper and lower tabs in the "home" position. The card may then be inserted and, as the card starts to engage the edge connector, firmly drive card home. Close down card cage locking tabs.

CAUTION

To ensure a stable and secure mating with the card edge connector when employing card extenders, card cage tabs must be in locked position.

a. Removal Remove spare track matrix as follows:

(1) Remove appropriate spare track select logic circuit card (fig. 3-6).

(2) Remove and retain two screws, lockwashers, washers, and spacers securing spare track matrix to spare track select logic circuit card.

(3) Remove spare track matrix.

b. Replacement. Install spare track matrix to the spare track select logic card using the screws, lockwashers and spaces retained in step a(2).

3-15. Front Panel Assembly

a. Removal. Remove front panel assembly as follows (fig. 3-5):

(1) Remove and retain 13 screws (2), one short screw (8), and 14 washers (3) securing front panel (9, fig. 3-5) to frame assembly.

NOTE

Install spare track selection matrix card in correct location; disc drive A on left, disc drive B on right.

(2) Remove front panel assembly.

b. Replacement. Install replacement front panel assembly using hardware removed in step a(11). Torque screws (2 and 8, fig. 3-5) to 18-inch pounds.

3-16. Handle

a. Removal Remove handle as follows:

(1) Remove two nuts and two lockwashers.

(2) Remove handle.

b. Replacement. Install replacement handle using two nuts and lockwashers removed in step a(l).

3-17. Slide Assembly

a. Removal. Remove slide assembly as follows:

(1) Refer to the Operator and Organizational Maintenance Manual TM 11-5805-683-12-1, Section II, for procedures to remove disc spindle assembly A and B, and power supply assembly.

(2) Remove card cage assembly as instructed in paragraph 3-13.

(3) Position frame assembly as shown in figure 3-7 and remove two screws securing frame assembly to slides.

(4) Pull frame assembly out fully and remove remaining 16 screws securing frame assembly to slides.

(5) Remove frame assembly.

(6) Remove slide assembly from cabinet.

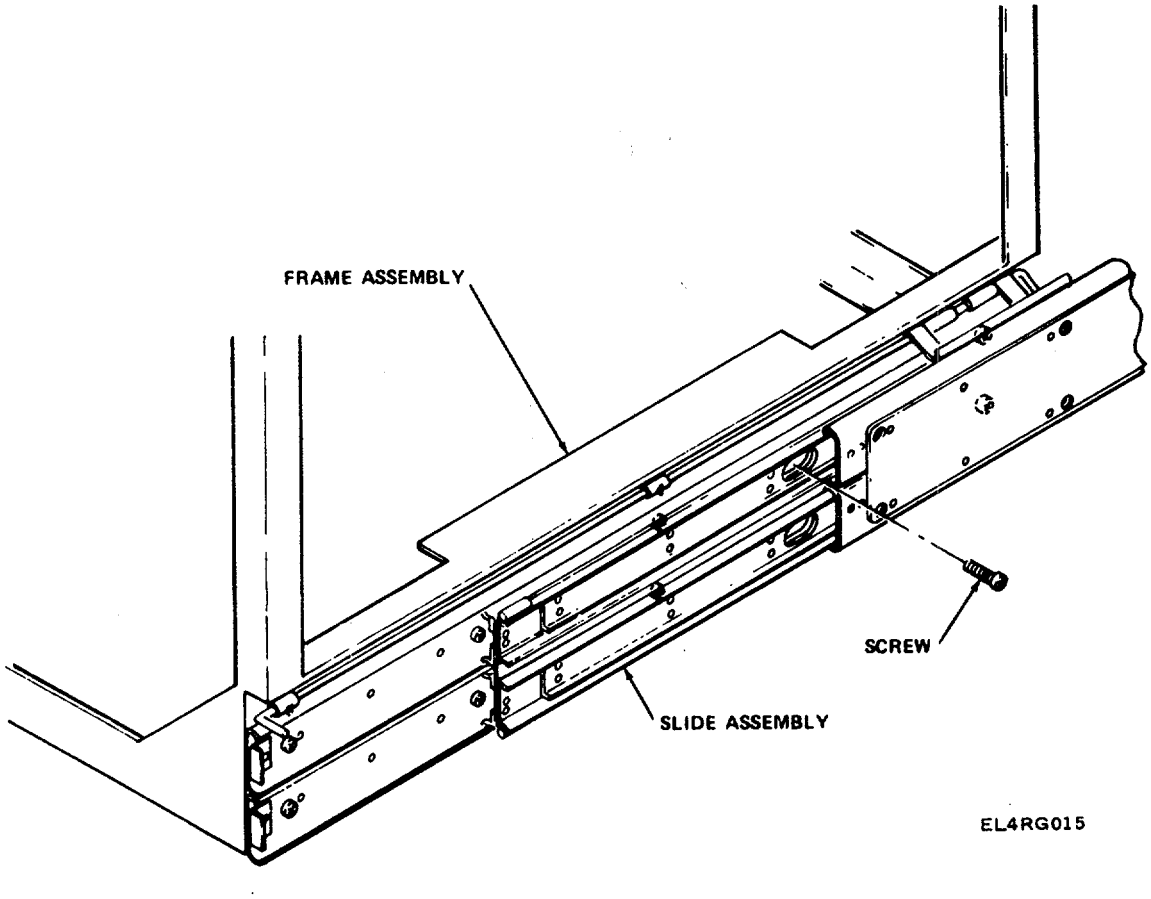


Figure 3-7. Slide Assembly Replacement

b. Replacement. Install replacement slide assembly to frame assembly as follows:

(1) Pull frame assembly out fully and install 16 screws, flat washers, lock washers removed in step a(4) above.

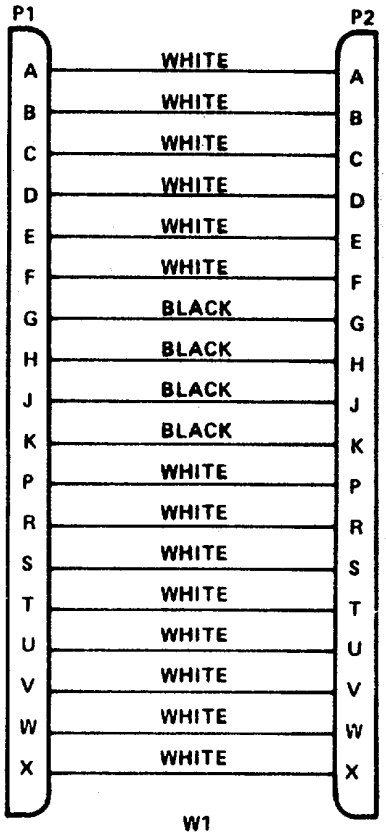
(2) Position frame assembly (fig. 3-7) and install two screws, flat washers, lock washers, and nuts removed in step a(3).

(3) Replace card cage as instructed in paragraph 3-13b.

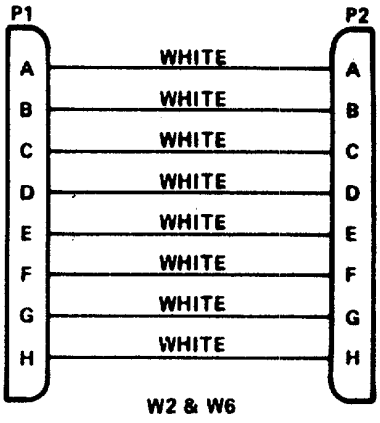
(4) Replace disc spindle assembly A and B and power supply as instructed in TM 11-5805-683-12-1, Section II.

3-18. Cable Assembly

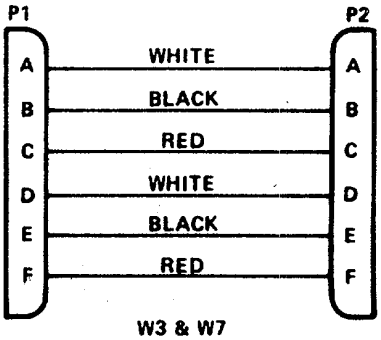
The RAS consists of nine interconnecting cables W1 through W9. Figure 3-8 provides cable length, plug identification, and pin-to-pin connection for continuity checks.



Cable Ref Des	Length (Inches)	P2 Ident	P2 Ident
W1	18 ± 0.5	W1 P1 A1 J1	W1 P2 A2 J2



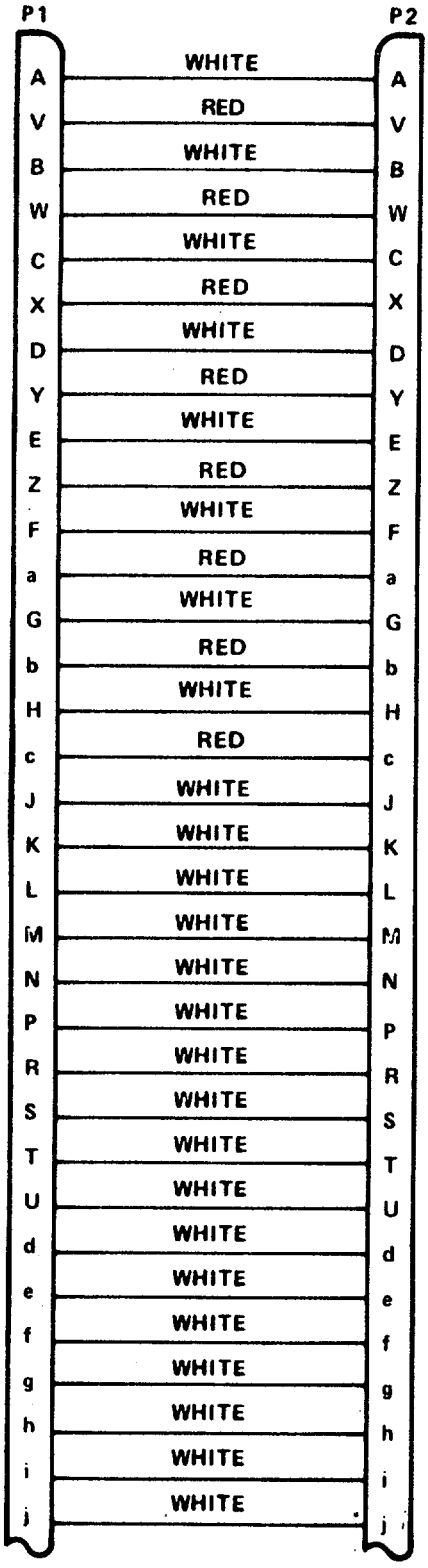
Cable Ref Des	Length (Inches)	P1 Ident	P2 Ident
W2	24 ± 0.5	W2 P1 A3 J4	W2 P2 A2 J3
W6	18 ± 0.5	W6 P1 A4 J4	W6 P2 A2 J4

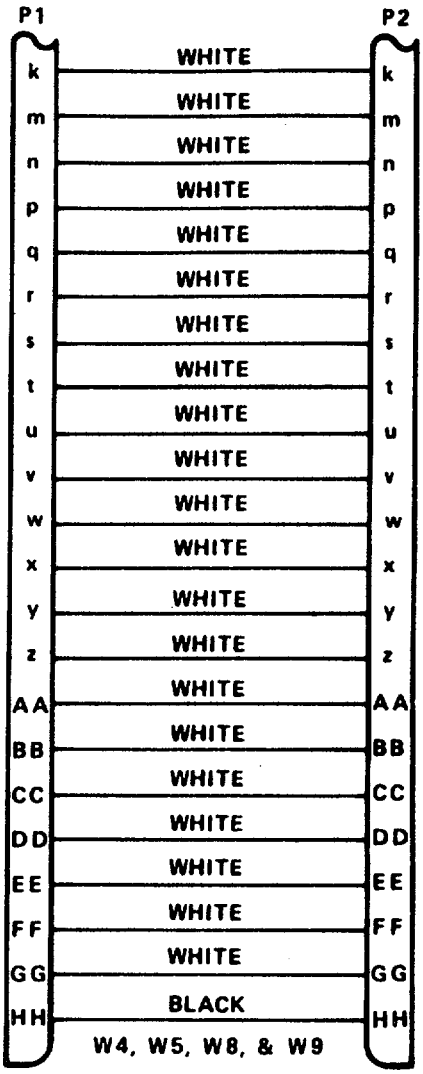


Cable Ref Des	Length (Inches)	P1 Ident	P2 Ident
W3	18 ± 0.5	W3 P1 A4 J3	W3 P2 A1 J9
W7	24 ± 0.5	W7 P1 A2 J3	W7 P2 A1 J8

EL4RG016

Figure 3-8. Cable Assembly Diagram (Sheet 1 of 2.





Cable Ref Des	Length (inches)	P1 Ident	P2 Ident
W4	24 ± 0.5	W4 P1 A4 J2	W4 P2 J1 J7
W5	24 ± 0.5	W5 P1 A4 J1	W5 P2 A1 J6
W8	30 ± 0.5	W8 P1 A3 J2	W8 P2 A1 J5
W9	30 ± 0.5	W9 P1 A3 J1	W9 P2 A1 J4

EL4RG017

Figure 3-8. Cable Assembly Diagram (Sheet 2 of 2).

3-19. Card Edge Connector Maintenance

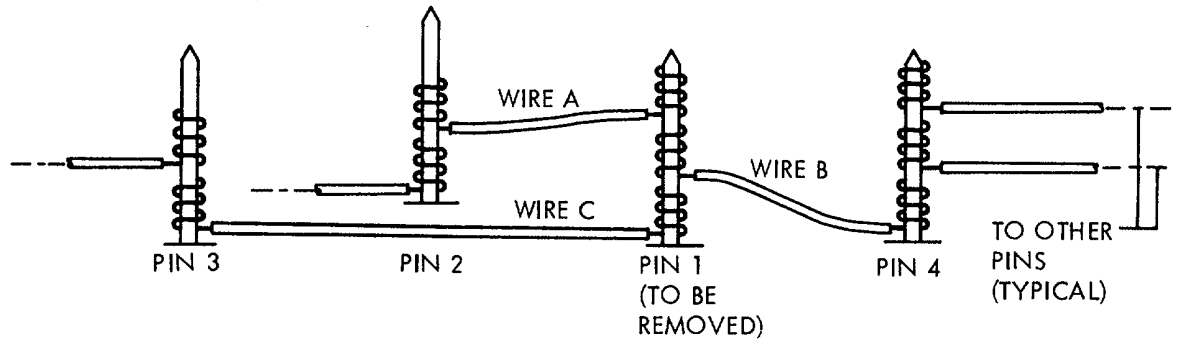
a. Pyramiding Wire Replacement. When new wiring must be installed, the degree of pyramiding must be determined before proceeding. The general restrictions are listed below.

(1) A wire that has been unwrapped cannot be rewrapped. If an adequate service loop is available, the wire can be clipped and rewrapped; if not, a new wire must be installed.

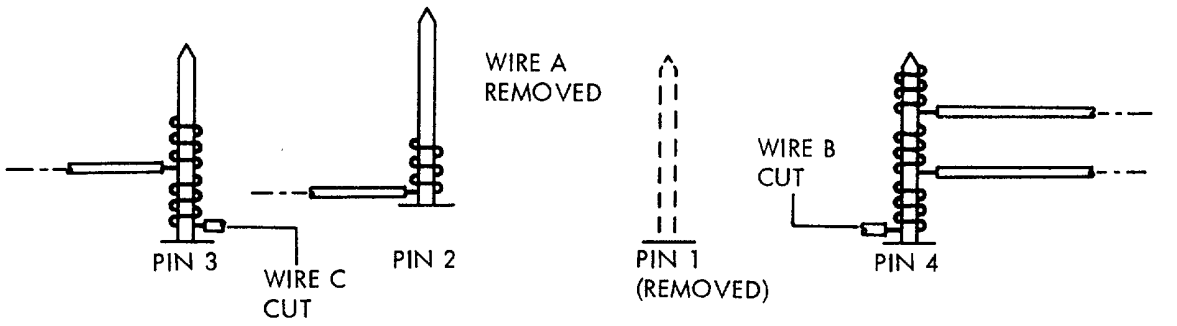
(2) No more than three wires can be wrapped on a single pin; a wire that has been clipped off and left in place counts as one of the three.

(3) Unwrapping a clipped wire and "sliding" the topmost wire(s) down is not permissible.

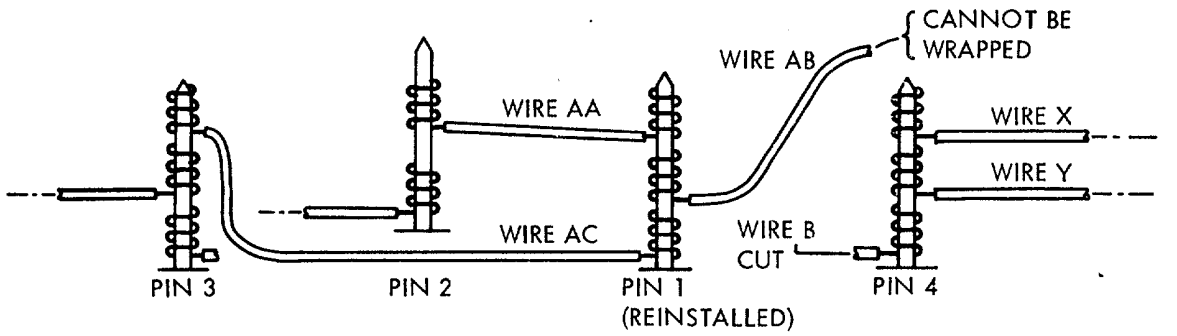
b. Wire Replacement Example. A wire replacement example is illustrated in figure 3-9 where a pin must be replaced as shown in example A. Wires A, B, and C must be removed to remove pin 1. Example B shows the wires removed; and example C shows the new wires (AA and AC) installed, with the exception of wire AB to pin 4. Since three connections are already in place (X, Y, and B cut-end), these three connections must be removed to permit wrapping wire AB. However, if wires X and Y were to be replaced, a pyramiding condition could be encountered where it may become impractical and too time-consuming to replace all other affected wires (i.e., all other wires related to wires X and Y replacement). A judgement is then necessary before starting to replace any wire, whether card edge connector repair or replacement should be undertaken.



EXAMPLE A.



EXAMPLE B.



EXAMPLE C.

EL4RG045

Figure 3-9. Pyramiding Wire Replacement Example.

c. Wire Wrap Post Removal. To remove a wire wrap post on one of the card edge connectors, proceed as follows:

(1) Using unwrap wire tool No. 26-32 AWG, remove and tag only those wires that are necessary to allow replacement of defective wire wrap post.

(2) Using extraction tool Teradyne No. 600-0001-000, remove defective wire wrap post by inserting tool over wire wrap post and gently tapping head of tool until post and nylon bushing fall free (fig. 3-10).

CAUTION

When extracting post and nylon bushing, make sure that both are recovered and do not fall into equipment. Discard post and bushing. DO NOT REUSE.

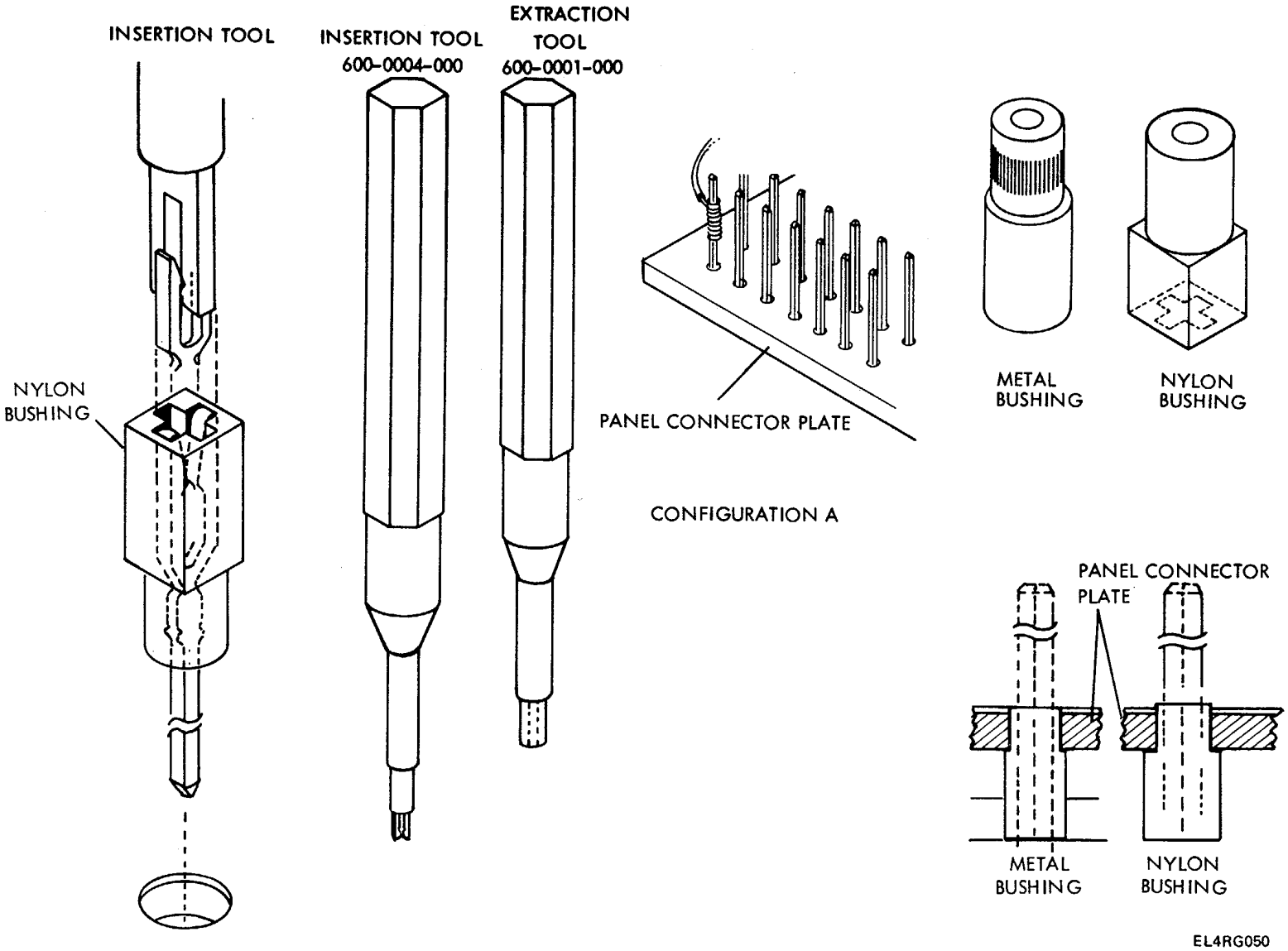


Figure 3-10. Typical Configurations For Wire Wrap Post Removal and Replacement.

d. Wire Wrap Post Replacement. To replace a wire wrap post, proceed as follows: CAUTION Do not insert bushing and post simultaneously.

(1) Insert nylon bushing into proper hole and gently tap bushing with insertion tool Teradyne No. 600-0004-000 for a snug press fit with bushing level with other bushings.

(2) Place post on insertion tool forks and insert into nylon bushing, making sure that post fork is oriented in same direction as all other posts. Ensure that post is in bushing by tapping until shoulder of tool strikes bushing.

(3) A removed wire should not be reused unless there is enough excess length to allow cutting off stripped end and restripping for wire wrapping. Replace entire wire if necessary using wire wrap gun NSN 5120-00-919-3486.

NOTE

More than one wire may have to be completely replaced when removing a wire wrap post.

3-20. Card Cage Connector J1 and J2

This paragraph provides procedures for removing and replacing the pins of connectors J 1 and J2.

NOTE

The crimping, positioning and insertion tools used in these procedures are part of the IL Wire Wrap/Connector Tool Kit.

a. J1 Pin Removal. To remove pins from connector J1, proceed as follows:

(1) Remove four nuts, four lockwashers, eight flat washers and four screws securing connector to card cage.

(2) Pull connector out of keyway.

(3) Tag all leads to connector pins.

NOTE

Remove all pins of faulty connector to avoid having one lead shorter than the others. A short lead places additional strain on a pin.

(4) Cut all leads to connector pins at top of crimp.

(5) Using removal tool MS24256R16, remove all pins from connector.

(6) Replace broken pin with an identical part, and reassemble connector in accordance with instructions in para 3-20 c.

b. J2 Pin Removal. To remove the pins from connector J2, proceed as follows:

(1) Remove four nuts, four lockwashers, eight flat washers and four screws securing J2 to card cage.

(2) Pull connector out of keyway.

(3) Tag all leads to connector pins.

NOTE

Remove all pins from faulty connector to avoid having one lead shorter than the others. A short lead places additional strain on a pin.

(4) Cut all leads to connector pins at top of crimp.

(5) Using removal tool MS24256R20, remove all pins from connector.

(6) Replace broken pin with an identical part, and reassemble connector in accordance with instructions in para 3-20d.

c. J1 Pin Replacement. To replace the pins of connector J 1, proceed as follows:

(1) Using crimping tool M2252011-01, crimp tagged leads to all replacement pins.

(2) Using positioning tool M22520/1-02 and insertion tool MS24256A16, insert pins into openings in connector indicated on tagged leads. Remove tags.

(3) Position connector in keyway, and secure connector with screws, washers and nuts removed as described in para 3-20 a, step (1).

d. J2 Pin Replacement. To replace pins of connector J2, proceed as follows:

(1) Using crimping tool M22520/1-01, crimp tagged leads to all replacement pins.

(2) Using positioning tool M22520/1-02 and insertion tool MS24256A20, insert pins into openings in connector indicated on tagged leads. Remove tags.

(3) Position connector in keyway, and secure connector with screws, washers, and nuts removed as described in para 3-20 b, step (1).

3-21. Cable Assembly Connector

The pins of the connectors on cable assemblies W1 through W9 are replaceable. This paragraph provides procedures for removing and replacing these pins.

NOTE

The crimping, positioning, and insertion tools used in these procedures are part of the IL Wire Wrap/Connector Tool Kit.

a. Connector Pin Removal (W3, W4, W5, W7, W8, W9). To remove the connector pins on these cable assemblies, proceed as follows: (1) Remove four nuts, four lockwashers, eight flat washers and four screws securing the connector to the assembly.

(2) Pull connector out of keyway.

(3) Tag all leads to connector pins.

NOTE

Remove all pins from connector to avoid having one lead shorter than the others. A short lead places additional strain on a pin.

(4) Cut all leads to the connector pins at top of crimp.

(5) Using removal tool MS3447-20, remove all pins from the connector.

(6) Replace broken pin with an identical part, and reassemble connector in accordance with instructions in para 3-20 c.

b. Connector Pin Removal (W1, W2, W6). To remove the connector pins on these cable assemblies, proceed as follows:

(1) Remove four nuts, four lockwashers, eight flat washers and four screws securing connector to assembly.

(2) Pull connector out of keyway.

(3) Tag all leads to connector pins.

(4) Cut all leads to connector pins.

NOTE

Remove all connector pins to avoid having one lead shorter than the others. A short lead places additional strain on a pin.

(5) Using removal tool MS3447-16, remove all pins from connector.

(6) Replace broken pin with an identical part, and reassemble connector in accordance with instructions in para 3-21 d.

c. Connector Pin Replacement (W3, W4, W5, W7, W8, W9). To replace the connector pins of these cable assemblies, proceed as follows:

(1) Using crimping tool M22520/1-01, crimp tagged leads to all replacement pins.

(2) Using positioning tool M22520/1-02 and insertion tool MS3447-20, insert pins into openings in connector indicated on tagged leads. Remove tags.

(3) Position connector in keyway, and secure connector with screws, flat washers, lock washers and nuts removed as described in para 3-21 a, step (1).

d. Connector Pin Replacement (W1, W2, W6). To replace the connector pins on these cable assemblies, proceed as follows:

(1) Using crimping tool M22520/1-01, crimp tagged leads to all replacement pins.

(2) Using insertion tool MS344716, insert pins into openings in connector indicated on tagged leads. Remove tags.

(3) Position connector in keyway, and secure connector with screws, flat washers, lock washers and nuts removed as described in para 3-21 b, step (1).

CHAPTER 4

GENERAL SUPPORT MAINTENANCE INSTRUCTIONS

General support maintenance consists of printed circuit card testing and repair, and power supply testing and repair. Refer to the Maintenance Allocation Chart (MAC) in TM-5805-683-12-1.

APPENDIX A
REFERENCES

DA Pam 310-1	Consolidated Index of Army Publications and Blank Forms
SB 11-573	Painting and Preservation Supplies Available for Field Use for Electronics Command Equipment
TM 11-5895-860-34P	Direct Support and General Support Repair Parts and Special Tool List:
EE640-CC-PLO-010/E154 RAS	Magnetic Disc, Data Storage, Random Access RD-491/TYC-39(V) (Including Depot RPSTL) (to be published)
TM 11-5805-683-12-1	Operator's and Organizational Maintenance Manual: Automatic
EE119-AA-OMI-010/E154 TYC39	Message Switching Central AN/TYC-39(V) (to be published)
T.O. 31W2-2TYC-39-1	
TM 11-6625-654-14	Operator's, Organizational, Direct Support and General Support Maintenance Repair Parts and Special Tools List (Including Depot Maintenance Repair Parts and Special Tools List) for Multimeter AN/USM-223 (to be published)
TM 11-6625-700-10	Operator's Manual Digital Readout, Electronic Counter ANIUSM-207 (NSN 6625-00-911-6368)
TM 11-6625-1541-15	Operator, Organizational, Direct Support, General Support, and Depot Maintenance Manual Hewlett-Packard RMS Vdtmeter Model 3400A (to be published)
TM 11-6625-2953-14	Operator's Organizational, Direct Support and General Support Maintenance Manual Multimeter AN/USM-451 (NSN 6625-01-060-68-4)
TM 11-6625-2735-14	Operator's, Organizational, Direct Support and General Support
0969-LP-170-1090	Maintenance Manual (Including Depot Maintenance) for Oscilloscope
T.O. 33A-13-498-1	OS-261/U (NSN 6625-00-127-0079)
TM 38-750	The Army Maintenance Management System (TAMMS) (to be published)
TM 740-90-1	Administrative Storage of Equipment
TM 746-10	Field Instructions for Painting and Preserving Electronics Command Equipment (to be published)

By Order of the Secretaries of the Army, the Navy, and the Air Force:

E. C. MEYER
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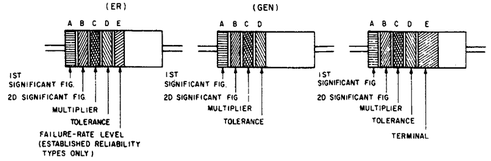


COLOR CODE MARKING FOR COMPOSITION TYPE RESISTORS.

COLOR-CODE MARKING FOR FILM-TYPE RESISTORS.

TABLE I
COLOR CODE FOR COMPOSITION TYPE AND FILM TYPE RESISTORS.

BAND A		BAND B		BAND C		BAND D		BAND E		
COLOR	FIRST SIGNIFICANT FIGURE	COLOR	SECOND SIGNIFICANT FIGURE	COLOR	MULTIPLIER	COLOR	RESISTANCE TOLERANCE (PERCENT)	COLOR	FAILURE RATE LEVEL	TERM.
BLACK	0	BLACK	0	BLACK	1			BROWN	M=1.0	
BROWN	1	BROWN	1	BROWN	10			RED	P=0.1	
RED	2	RED	2	RED	100			ORANGE	R=0.01	
ORANGE	3	ORANGE	3	ORANGE	1,000			YELLOW	S=0.001	
YELLOW	4	YELLOW	4	YELLOW	10,000	SILVER	±10 (COMP. TYPE ONLY)	WHITE		SOLDERABLE
GREEN	5	GREEN	5	GREEN	100,000	GOLD	±5			
BLUE	6	BLUE	6	BLUE	1,000,000	RED	±2 (NOT APPLICABLE TO ESTABLISHED RELIABILITY)			
PURPLE (VIOLET)	7	PURPLE (VIOLET)	7							
GRAY	8	GRAY	8	SILVER	0.01					
WHITE	9	WHITE	9	GOLD	0.1					

BAND A — THE FIRST SIGNIFICANT FIGURE OF THE RESISTANCE VALUE (BANDS A THRU D SHALL BE OF EQUAL WIDTH.)

BAND B — THE SECOND SIGNIFICANT FIGURE OF THE RESISTANCE VALUE.

BAND C — THE MULTIPLIER (THE MULTIPLIER IS THE FACTOR BY WHICH THE TWO SIGNIFICANT FIGURES ARE MULTIPLIED TO YIELD THE NOMINAL RESISTANCE VALUE.)

BAND D — THE RESISTANCE TOLERANCE.

BAND E — WHEN USED ON COMPOSITION RESISTORS, BAND E INDICATES ESTABLISHED RELIABILITY FAILURE-RATE LEVEL (PERCENT FAILURE PER 1,000 HOURS) ON FILM RESISTORS, THIS BAND SHALL BE APPROXIMATELY 1-1/2 TIMES THE WIDTH OF OTHER BANDS, AND INDICATES TYPE OF TERMINAL.

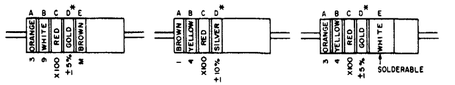
RESISTANCES IDENTIFIED BY NUMBERS AND LETTERS (THESE ARE NOT COLOR CODED.)

SOME RESISTORS ARE IDENTIFIED BY THREE OR FOUR DIGIT ALPHA NUMERIC DESIGNATORS. THE LETTER R IS USED IN PLACE OF A DECIMAL POINT WHEN FRACTIONAL VALUES OF AN OHM ARE EXPRESSED. FOR EXAMPLE:

2R7 = 2.7 OHMS 10R0 = 10.0 OHMS

FOR WIRE-WOUND-TYPE RESISTORS COLOR CODING IS NOT USED, IDENTIFICATION MARKING IS SPECIFIED IN EACH OF THE APPLICABLE SPECIFICATIONS.

EXAMPLES OF COLOR CODING



NOMINAL RESISTANCE 3,900 OHMS
RESISTANCE TOLERANCE ±5%
FAILURE RATE LEVEL M

NOMINAL RESISTANCE 1,400 OHMS
RESISTANCE TOLERANCE ±10%

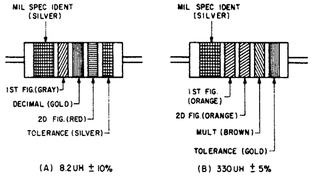
NOMINAL RESISTANCE 3,400 OHMS
RESISTANCE TOLERANCE ±5%
TERMINAL SOLDERABLE

COMPOSITION-TYPE RESISTORS

FILM-TYPE RESISTORS

* IF BAND D IS OMITTED, THE RESISTOR TOLERANCE IS ±20% AND THE RESISTOR IS NOT MIL-STD.

A. COLOR CODE MARKING FOR MILITARY STANDARD RESISTORS.



(A) 8.2UH ± 10%

(B) 330UH ± 5%

COLOR CODING FOR TUBULAR ENCAPSULATED R.F. CHOKES. AT A, AN EXAMPLE OF OF THE CODING FOR AN 8.2UH CHOKE IS GIVEN AT B, THE COLOR BANDS FOR A 330UH INDUCTOR ARE ILLUSTRATED.

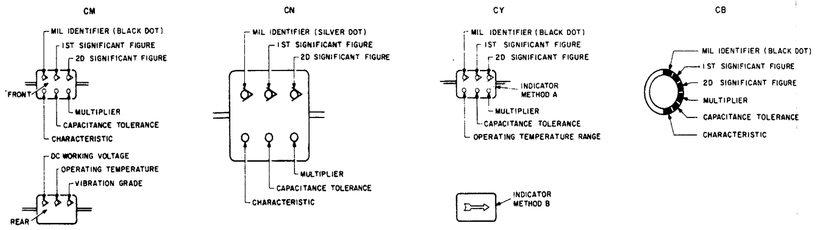
TABLE 2
COLOR CODING FOR TUBULAR ENCAPSULATED R.F. CHOKES.

COLOR	SIGNIFICANT FIGURE	MULTIPLIER	INDUCTANCE TOLERANCE (PERCENT)
BLACK	0	1	
BROWN	1	10	1
RED	2	100	2
ORANGE	3	1,000	3
YELLOW	4		
GREEN	5		
BLUE	6		
VIOLET	7		
GRAY	8		
WHITE	9		
NONE			20
SILVER			10
GOLD	DECIMAL POINT		5

MULTIPLIER IS THE FACTOR BY WHICH THE TWO COLOR FIGURES ARE MULTIPLIED TO OBTAIN THE INDUCTANCE VALUE OF THE CHOKE COIL.

B. COLOR CODE MARKING FOR MILITARY STANDARD INDUCTORS.

CAPACITORS, FIXED, VARIOUS-DIELECTRICS, STYLES CM, CN, CY, AND CB.

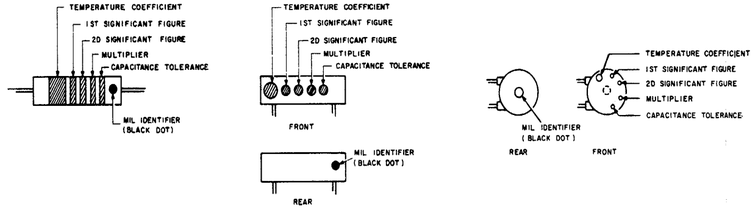


MICA-DIELECTRIC

PAPER-DIELECTRIC

GLASS-DIELECTRIC, GLASS CASE

MICA, BUTTON TYPE



AXIAL LEAD

RADIAL LEAD

DISK-TYPE

C. COLOR CODE MARKING FOR MILITARY STANDARD CAPACITORS.

TABLE 3 — FOR USE WITH STYLES CM, CN, CY AND CB.

COLOR	MIL ID	1ST SIG FIG.	2D SIG FIG	MULTIPLIER[1]	CAPACITANCE TOLERANCE				CHARACTERISTIC[2]			DC WORKING VOLTAGE	OPERATING TEMP. RANGE	VIBRATION GRADE
					CM	CN	CY	CB	CM	CN	CB	CM	CY, CM	CM
BLACK	CM, CY, CB	0	0	1			±20%	±20%		A			-55°TO+70°C	10-55 HZ
BROWN		1	1	10					B	E	B			
RED		2	2	100	±2%		±2%	±2%	C				-55°TO+85°C	
ORANGE		3	3	1,000		±30%			D		D	300		
YELLOW		4	4	10,000					E				-55°TO+125°C	10-2,000HZ
GREEN		5	5		±5%				F			500		
BLUE		6	6										-55°TO+150°C	
PURPLE (VIOLET)		7	7											
GRAY		8	8											
WHITE		9	9											
GOLD				0.1			±5%	±5%						
SILVER	CN			0.01	±10%	±10%	±10%	±10%						

TABLE 4 — TEMPERATURE COMPENSATING, STYLE CC.

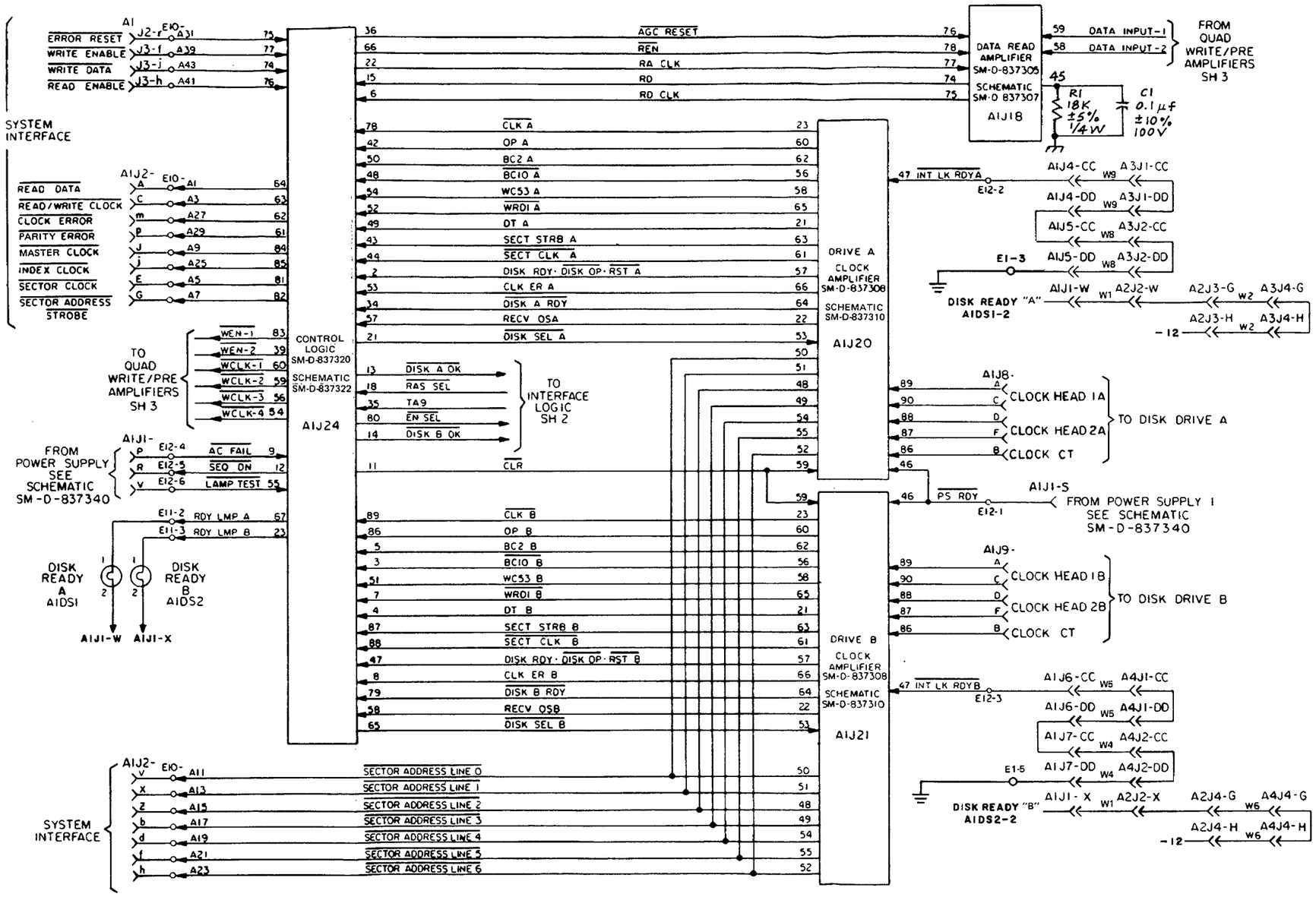
COLOR	TEMPERATURE COEFFICIENT[4]	1ST SIG FIG.	2D SIG FIG.	MULTIPLIER[1]	CAPACITANCE TOLERANCE		MIL ID
					CAPACITANCES OVER 10 UUF	CAPACITANCES 10 UUF OR LESS	
BLACK	0	0	0	1		±2.0 UUF	CC
BROWN	-30	1	1	10	±1%		
RED	-80	2	2	100	±2%	±0.25 UUF	
ORANGE	-150	3	3	1,000			
YELLOW	-220	4	4				
GREEN	-330	5	5		±5%	±0.5 UUF	
BLUE	-470	6	6				
PURPLE (VIOLET)	-750	7	7				
GRAY		8	8	0.01*			
WHITE		9	9	0.1*	±10%		
GOLD	+100			0.1		±1.0 UUF	
SILVER				0.01			

1. THE MULTIPLIER IS THE NUMBER BY WHICH THE TWO SIGNIFICANT (SIG) FIGURES ARE MULTIPLIED TO OBTAIN THE CAPACITANCE IN UUF.
2. LETTERS INDICATE THE CHARACTERISTICS DESIGNATED IN APPLICABLE SPECIFICATIONS: MIL-C-5, MIL-C-25D, MIL-C-11272B, AND MIL-C-10950C RESPECTIVELY.
3. LETTERS INDICATE THE TEMPERATURE RANGE AND VOLTAGE-TEMPERATURE LIMITS DESIGNATED IN MIL-C-11015D.
4. TEMPERATURE COEFFICIENT IN PARTS PER MILLION PER DEGREE CENTIGRADE.

* OPTIONAL CODING WHERE METALLIC PIGMENTS ARE UNDESIRABLE.

EL4RG018

Figure FO-1. Standard Color Coding Chart



NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. PREFIX THE DESIGNATION(S) WITH ASSEMBLY DESIGNATION.
2. REF DWG NO: ASSEMBLY DWG SM-D-837300.
3. FOR SYSTEM CABLE INTERCONNECT DIAGRAM SEE SM-D-837526.
4. ARROWHEADS DENOTE SIGNAL FLOW.
5. FOR HARNESS DRAWING OF CARD CAGE (A1) SEE SM-D-837529 AND WIRE LIST SM-D-837530.
6. FOR LOGIC DIAGRAM OF DISK DRIVE A AND B (A3 AND A4) SEE SM-D-837348.
7. SUBASSEMBLY REFERENCE DESIGNATION: A1 IS CARD CAGE ASSEMBLY SM-D-837302, A2 IS POWER SUPPLY ASSEMBLY SM-D-837588, A3 IS DISK DRIVE A, A4 IS DISK DRIVE B ASSEMBLIES SM-D-837301.

EL4RG019

Figure FO-2. System Interconnection Schematic Diagram (Sheet 1 of 3)
Change 1

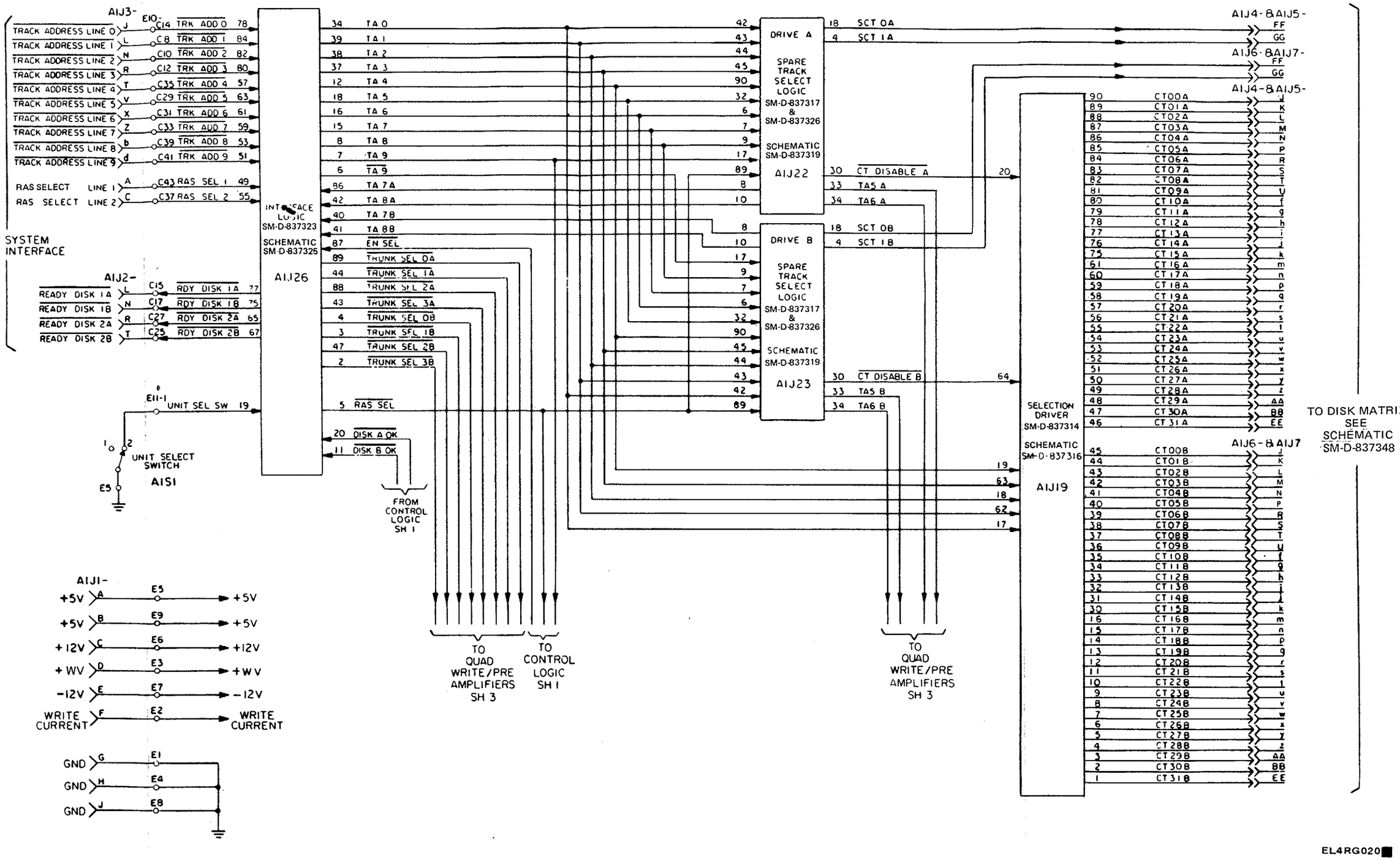


Figure FO-2. System Interconnection Schematic Diagram (Sheet 2 of 3)
Change 1

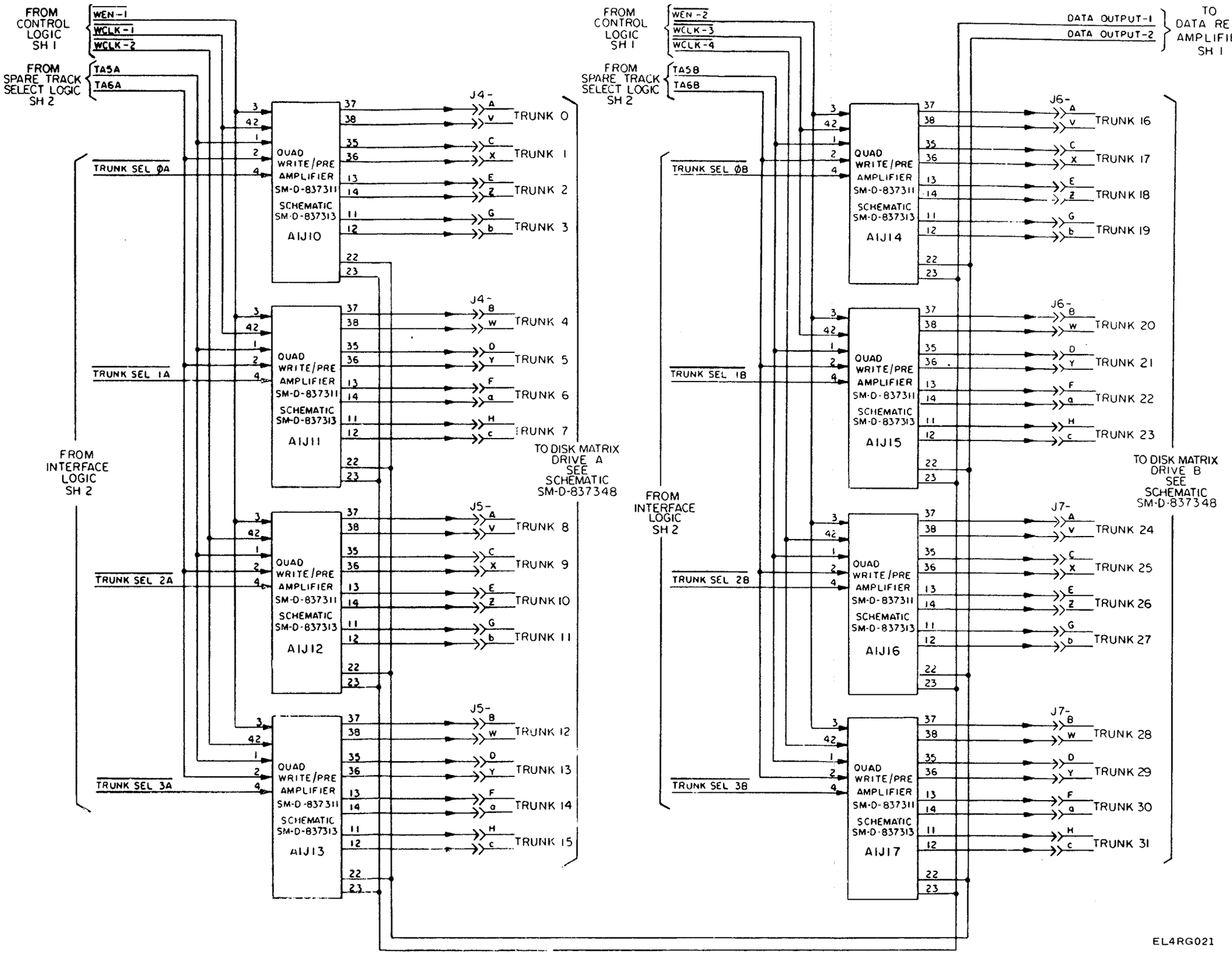
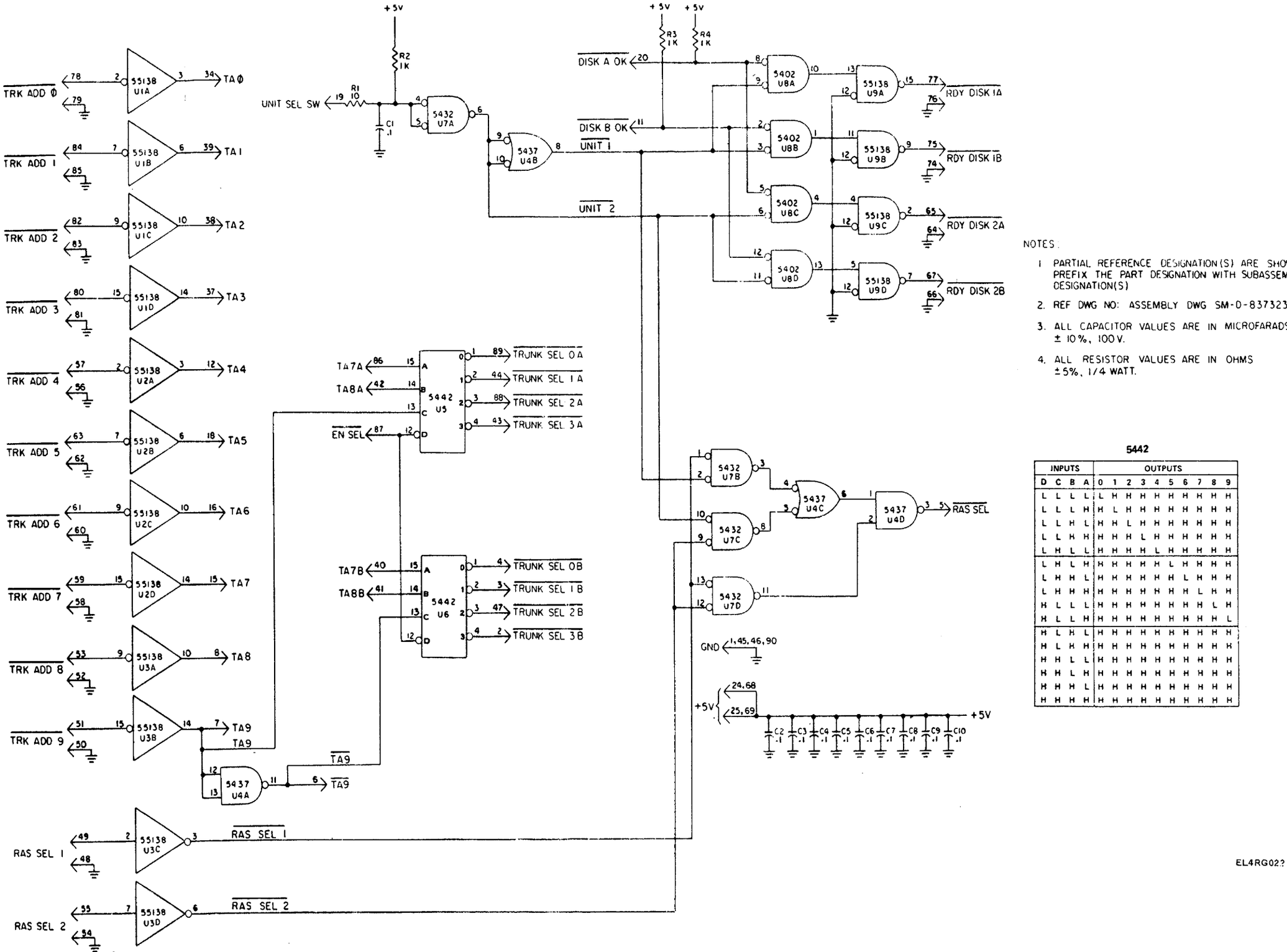


Figure FO-2. System Interconnection Schematic Diagram (Sheet 3 of 3)



NOTES:

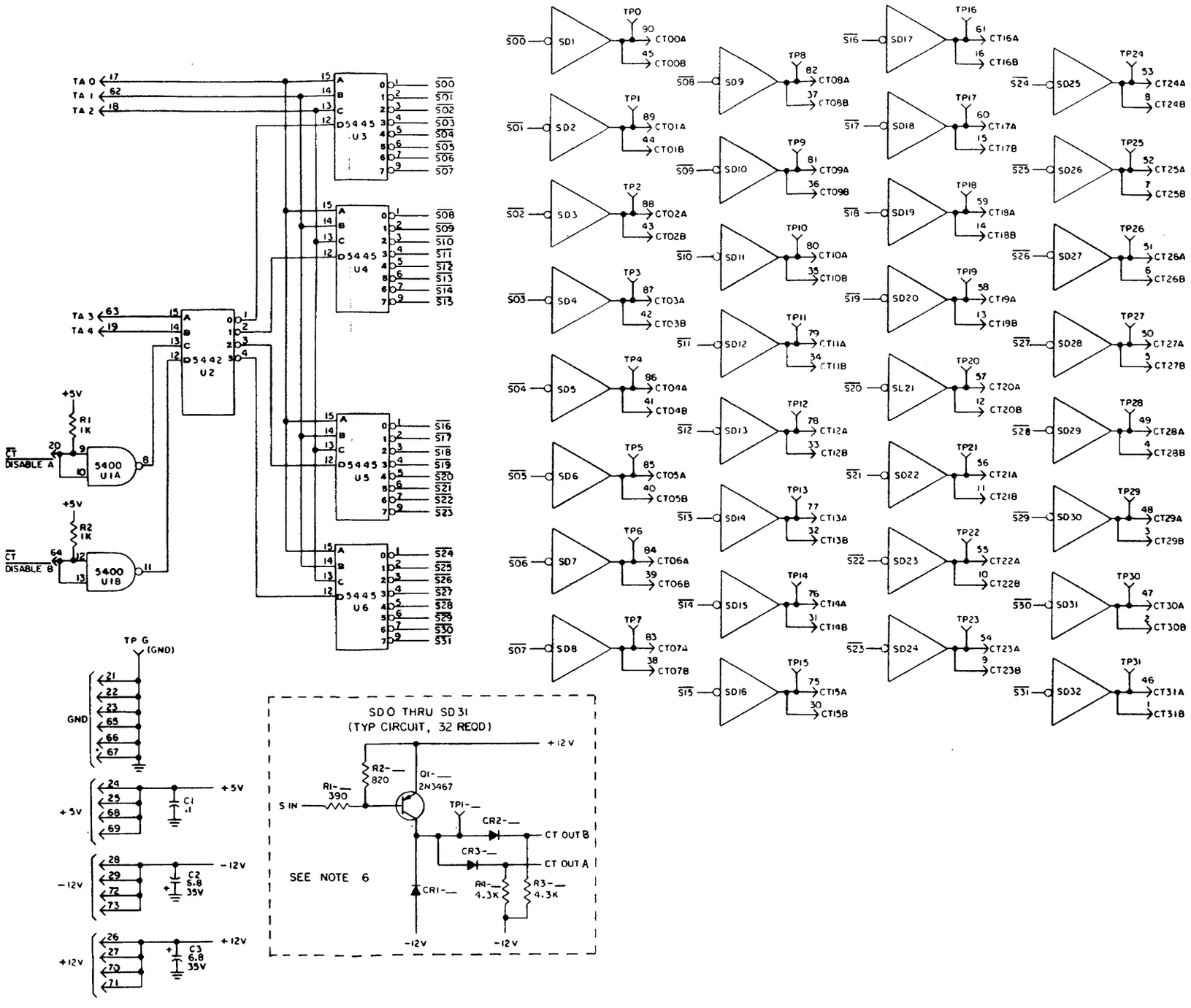
1. PARTIAL REFERENCE DESIGNATION(S) ARE SHOWN PREFIX THE PART DESIGNATION WITH SUBASSEMBLY DESIGNATION(S)
2. REF DWG NO: ASSEMBLY DWG SM-D-837323.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS ± 10%, 100 V.
4. ALL RESISTOR VALUES ARE IN OHMS ±5%, 1/4 WATT.

5442

INPUTS				OUTPUTS									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

EL4RG02?

Figure FO-3. Interface Logic Diagram



NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. PREFIX THE PART DESIGNATION WITH SUBASSEMBLY DESIGNATION.
2. REF DWG NO: ASSEMBLY DWG SM-D-837314.
3. ALL RESISTOR VALUES ARE IN OHMS ±5%, 1/4W.
4. ALL CAPACITOR VALUES ARE IN MICROFARADS ±10%, 35V.
5. ALL DIODES ARE JAN1N4148.
6. COMPONENT DESIGNATIONS ARE FOLLOWED BY SELECTION DRIVER NUMBER. EXAMPLE Q1 - 0 THRU Q1 - 31.

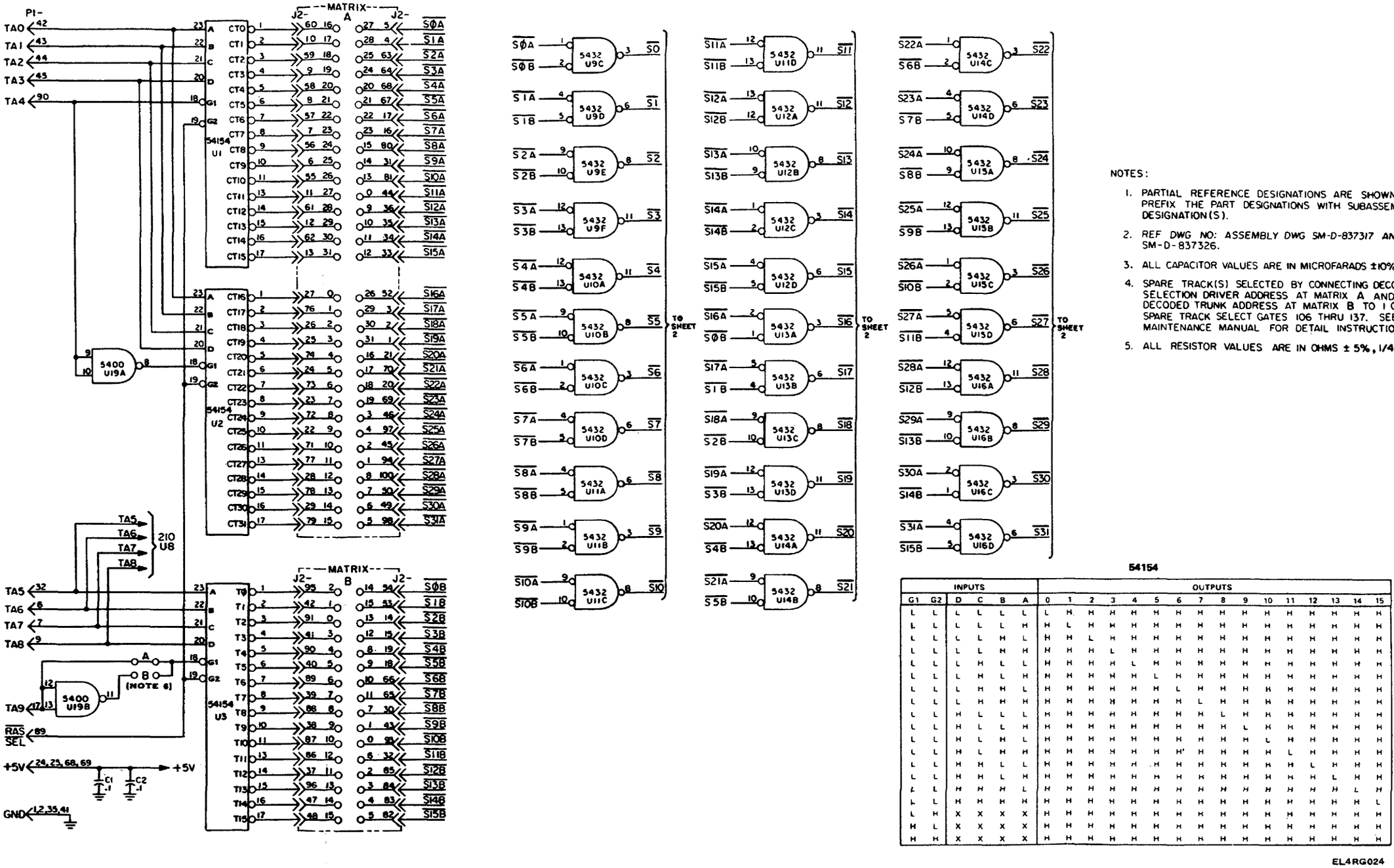
5442/5445

INPUTS				OUTPUTS									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

EL4RG023

Figure FO-4. Selection Driver Schematic Diagram.

Change 1



NOTES:

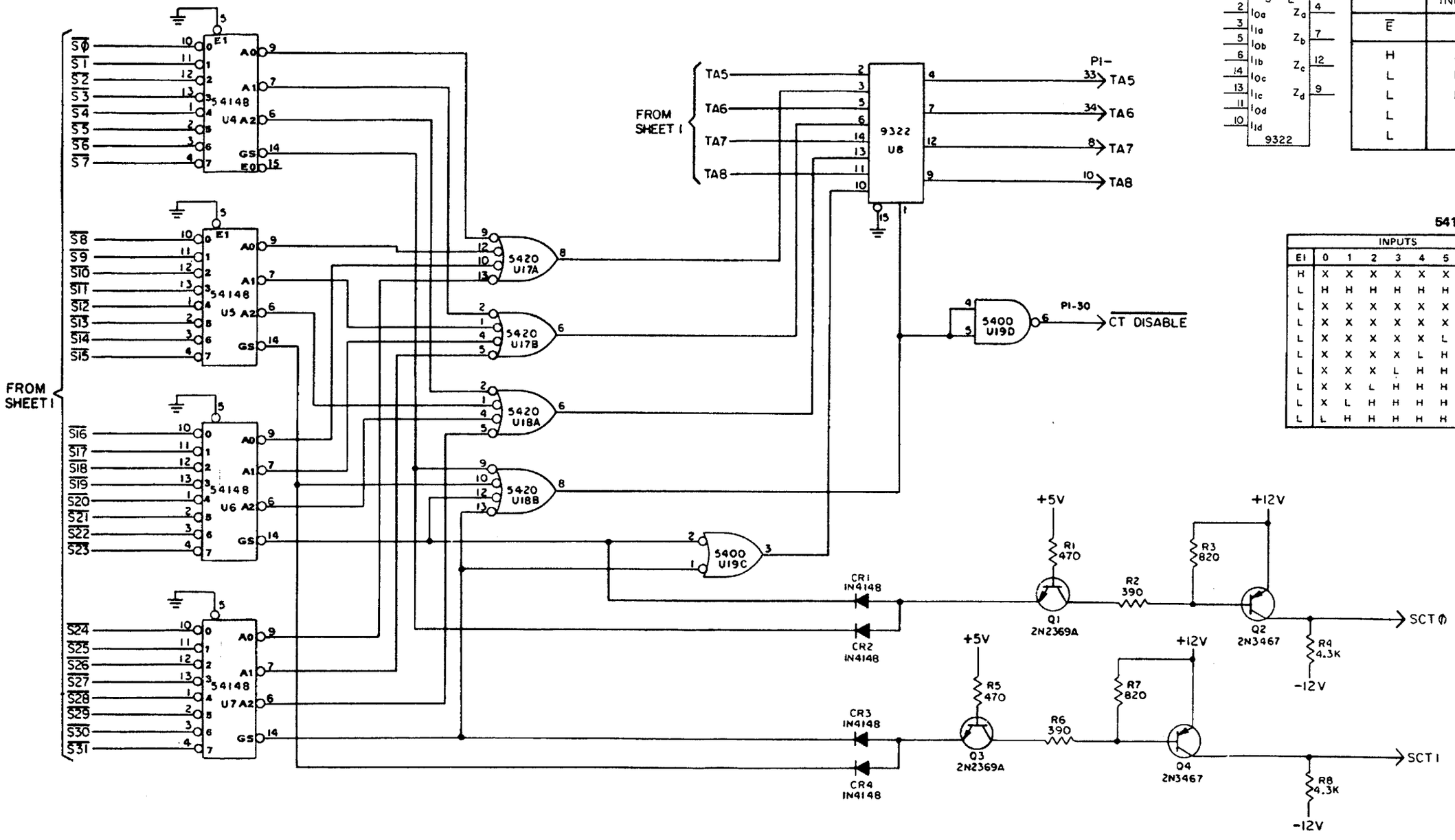
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. PREFIX THE PART DESIGNATIONS WITH SUBASSEMBLY DESIGNATION(S).
2. REF DWG NO: ASSEMBLY DWG SM-D-837317 AND SM-D-837326.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS ±10%,100V.
4. SPARE TRACK(S) SELECTED BY CONNECTING DECODED SELECTION DRIVER ADDRESS AT MATRIX A AND DECODED TRUNK ADDRESS AT MATRIX B TO 1 OF 32 SPARE TRACK SELECT GATES 106 THRU 137. SEE MAINTENANCE MANUAL FOR DETAIL INSTRUCTIONS.
5. ALL RESISTOR VALUES ARE IN OHMS ± 5%, 1/4 W.

54154

INPUTS						OUTPUTS													
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

EL4RG024

Figure FO-5. Spare Track Select Logic Diagram (Sheet 1 of 2).



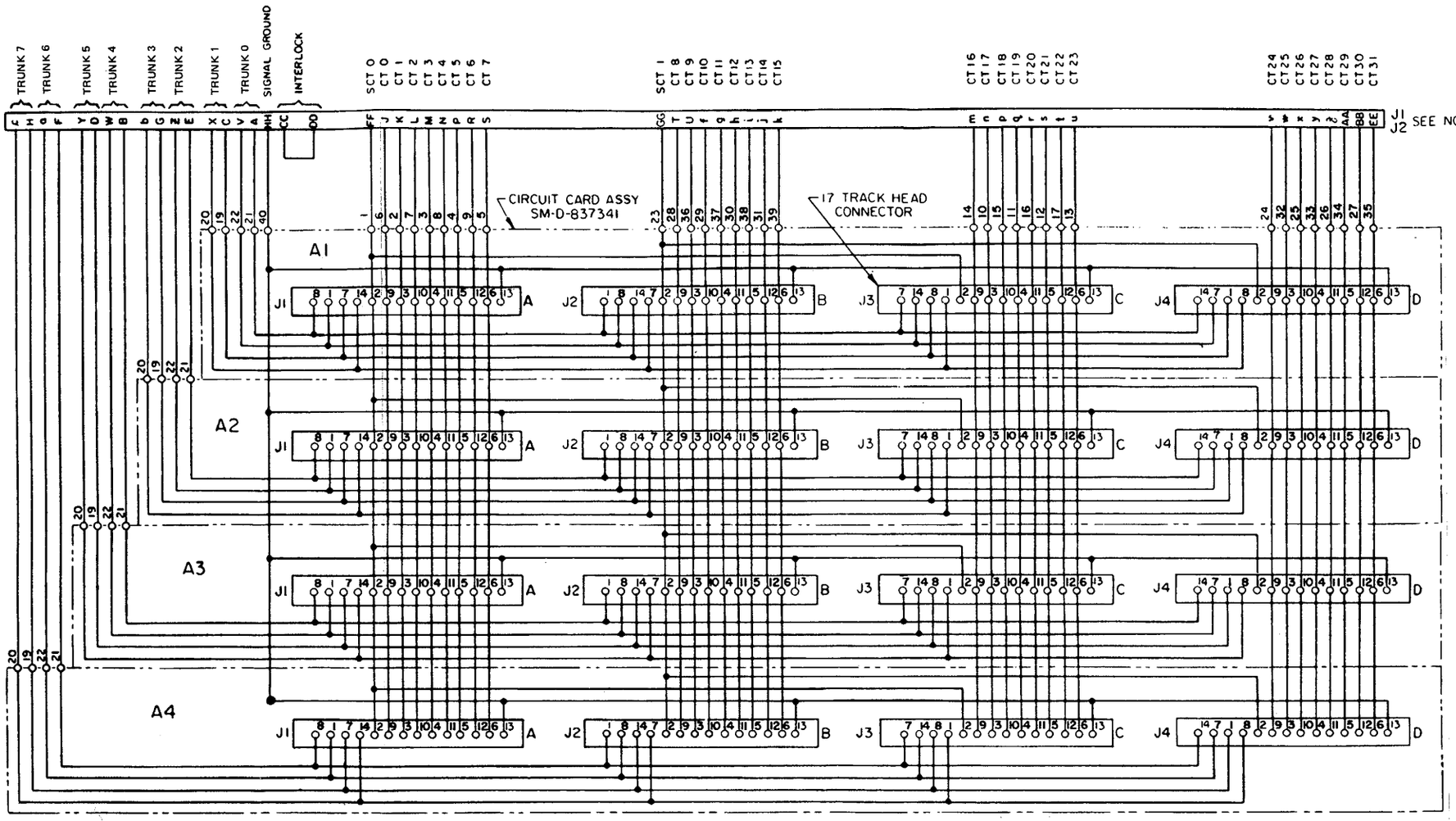
9322

ENABLE	SELECT INPUT	INPUTS		OUTPUT
$\overline{E}$	S	I_{0X}	I_{1X}	Z_X
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

54148

INPUTS								OUTPUTS				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

Figure FO-5. Spare Track Select Logic Diagram (Sheet 2 of 2).

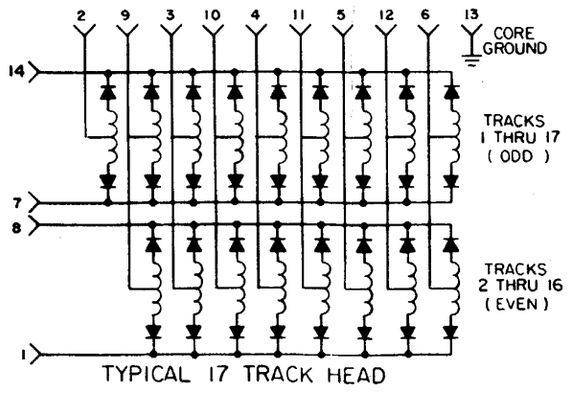


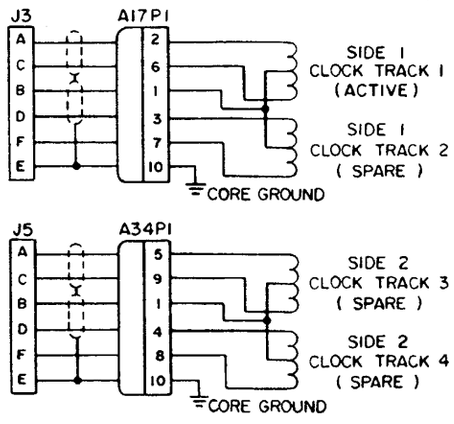
NOTES:

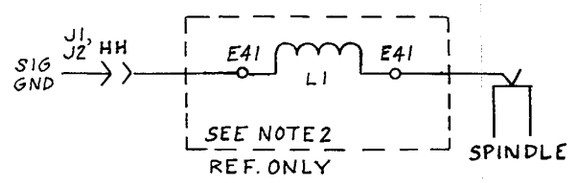
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, PREFIX THE DESIGNATION(S) WITH SUBASSEMBLY DESIGNATION.
2. REF DWG NO. ASSEMBLY DWG SM-D-837301.
3. DIODES ARE JAN1N4150-1.
4. FOR HARNESS SEE DWGS SM-D-837347, SM-D-837398.
5. WIRING FOR 256 TRACK SHOWN, EACH 512 TRACK DISK ASSEMBLY CONTAINS TWO SUCH MATRICES (J1 AND J2).

MATRIX HEAD CONNECTION CHART SIDE 1 / SIDE 2

	A	B	C	D
A1	A6 / A31	A14 / A23	A5 / A30	A13 / A22
A2	A4 / A29	A12 / A21	A3 / A28	A11 / A20
A3	A2 / A27	A10 / A19	A1 / A26	A9 / A18
A4	A8 / A33	A16 / A25	A7 / A32	A15 / A24



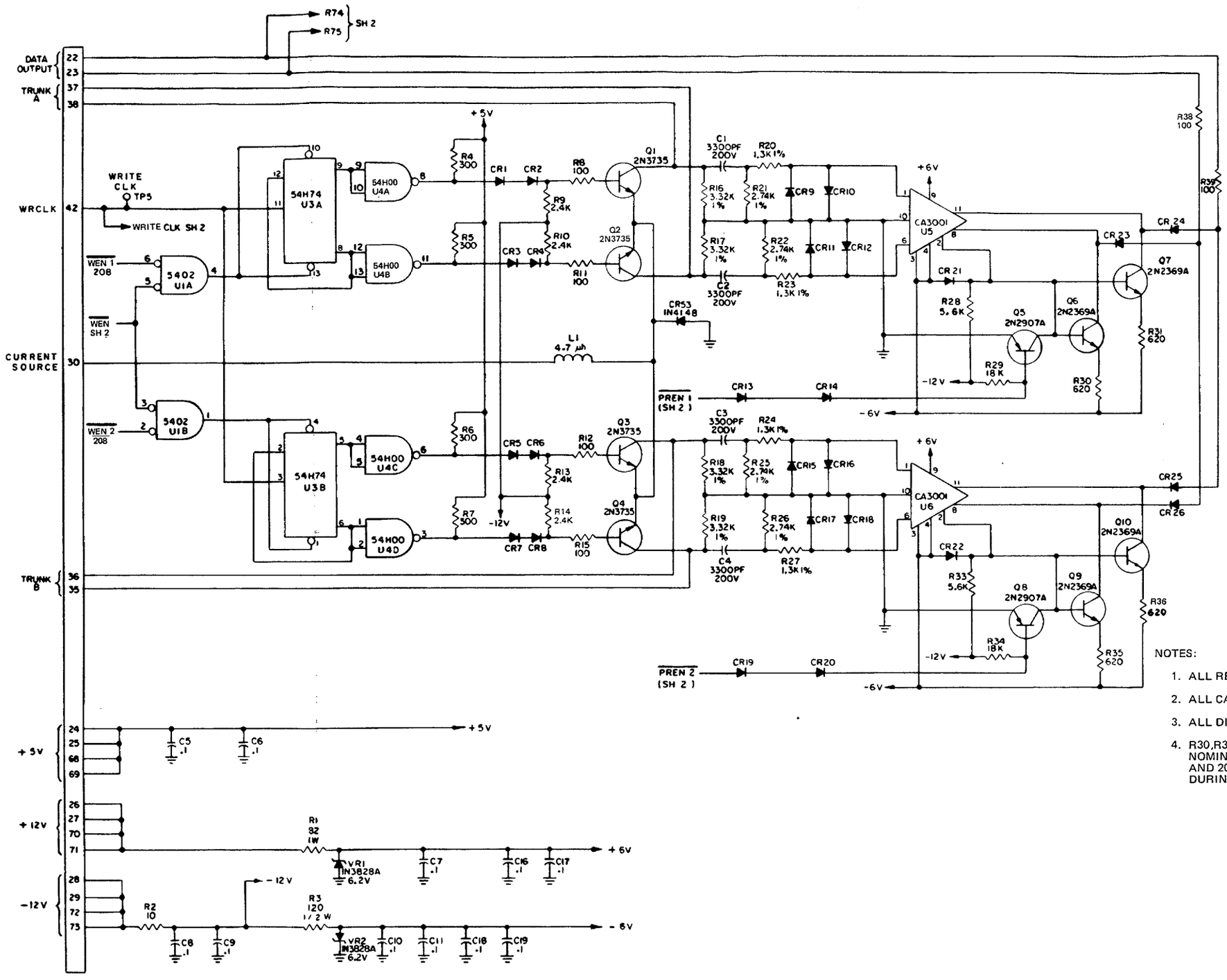




EL4RG026

Figure FO-6. Matrix Interconnect Schematic Diagram.

Change 1



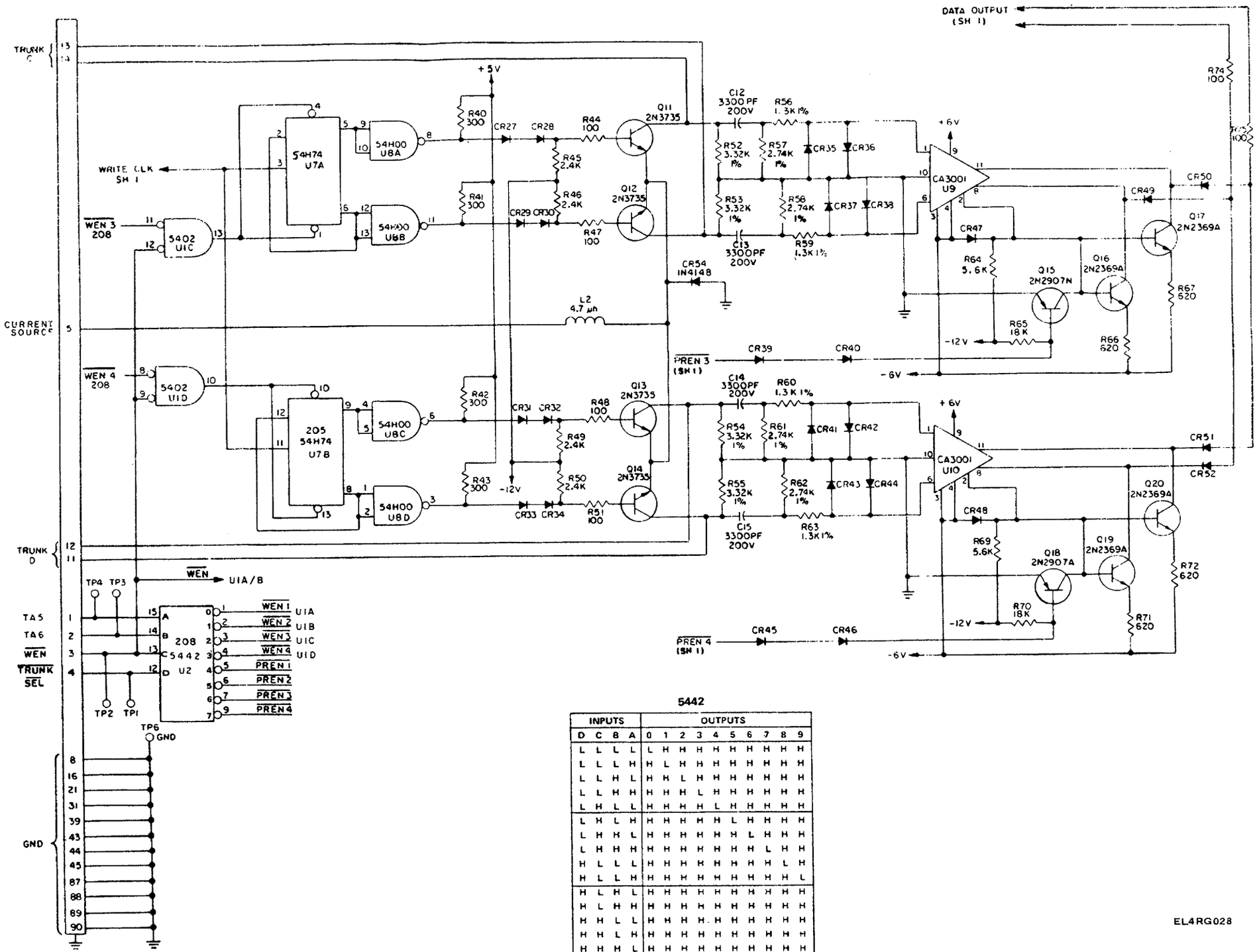
NOTES:

1. ALL RESISTOR VALUES ARE GIVEN IN OHMS, ±5%, 1/4W.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS, 100V ± 10%.
3. ALL DIODES ARE 1N4532.
4. R30,R31,R35,R36,R66,R67,R71,R72 ARE 620 OHMS NOMINAL. SELECTION RANGE BETWEEN 1.2K MAX. AND 200 OHMS MIN. TO MATCH PREAMP OUTPUT DURING TEST.

EL4RG027

Figure FO-7. Quad Write/Preamplifier Schematic Diagram (Sheet 1 of 2).

Change 1

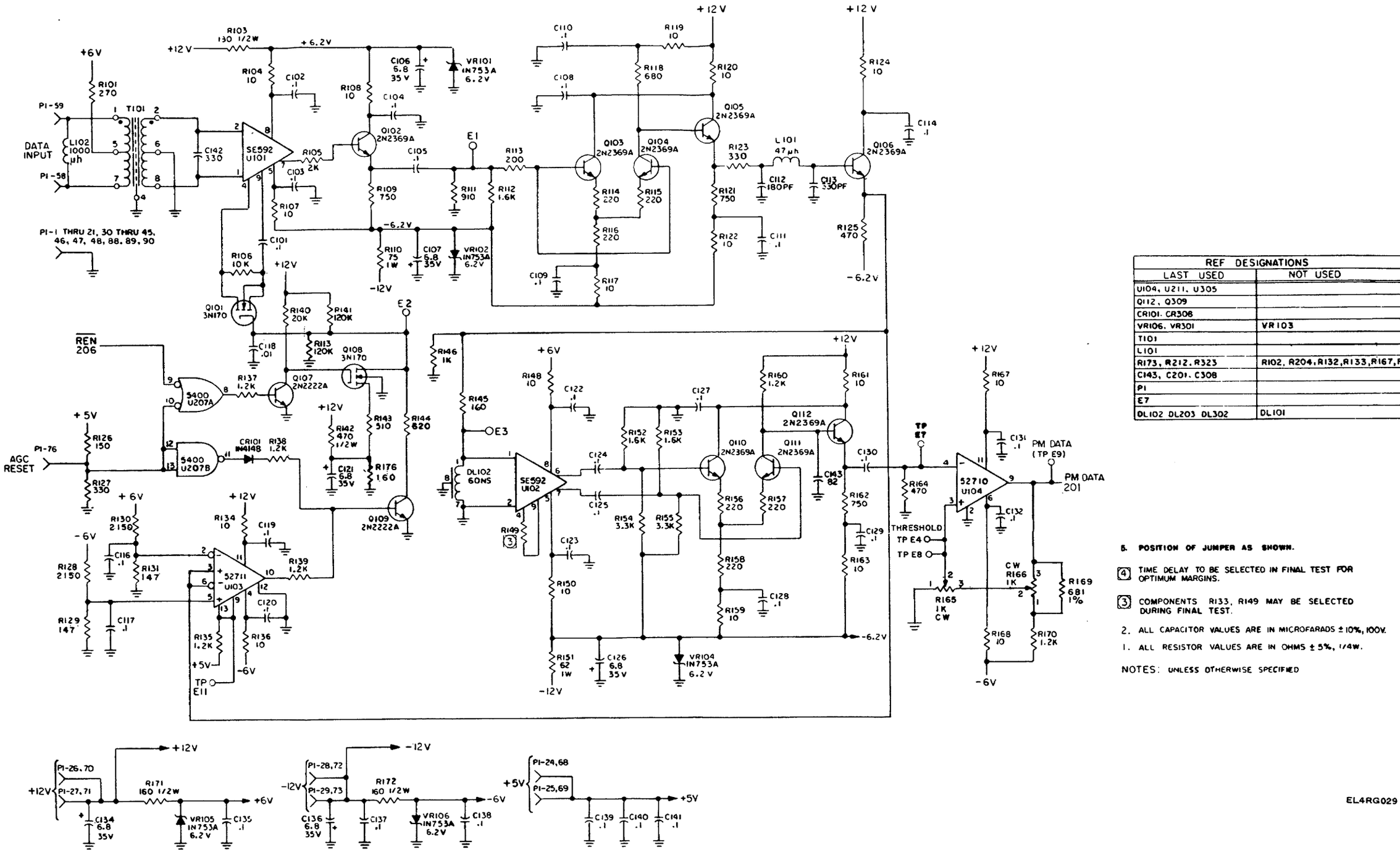


5442

INPUTS				OUTPUTS									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

EL4RG028

Figure FO-7. Quad Write/Preamplifier Schematic Diagram (Sheet 2 of 2).



REF DESIGNATIONS	
LAST USED	NOT USED
U104, U211, U305	
Q112, Q309	
CR101, CR308	
VR106, VR301	VR103
T101	
L101	
R173, R212, R323	R102, R204, R132, R133, R167, R166
C143, C201, C308	
P1	
E7	
DL102 DL203 DL302	DL101

5. POSITION OF JUMPER AS SHOWN.

(4) TIME DELAY TO BE SELECTED IN FINAL TEST FOR OPTIMUM MARGINS.

(3) COMPONENTS R133, R149 MAY BE SELECTED DURING FINAL TEST.

2. ALL CAPACITOR VALUES ARE IN MICROFARADS ± 10%, 100V.

1. ALL RESISTOR VALUES ARE IN OHMS ± 5%, 1/4W.

NOTES: UNLESS OTHERWISE SPECIFIED

EL4RG029

Figure FO-8. Data Read Amplifier Schematic Diagram (Sheet 1 of 3)

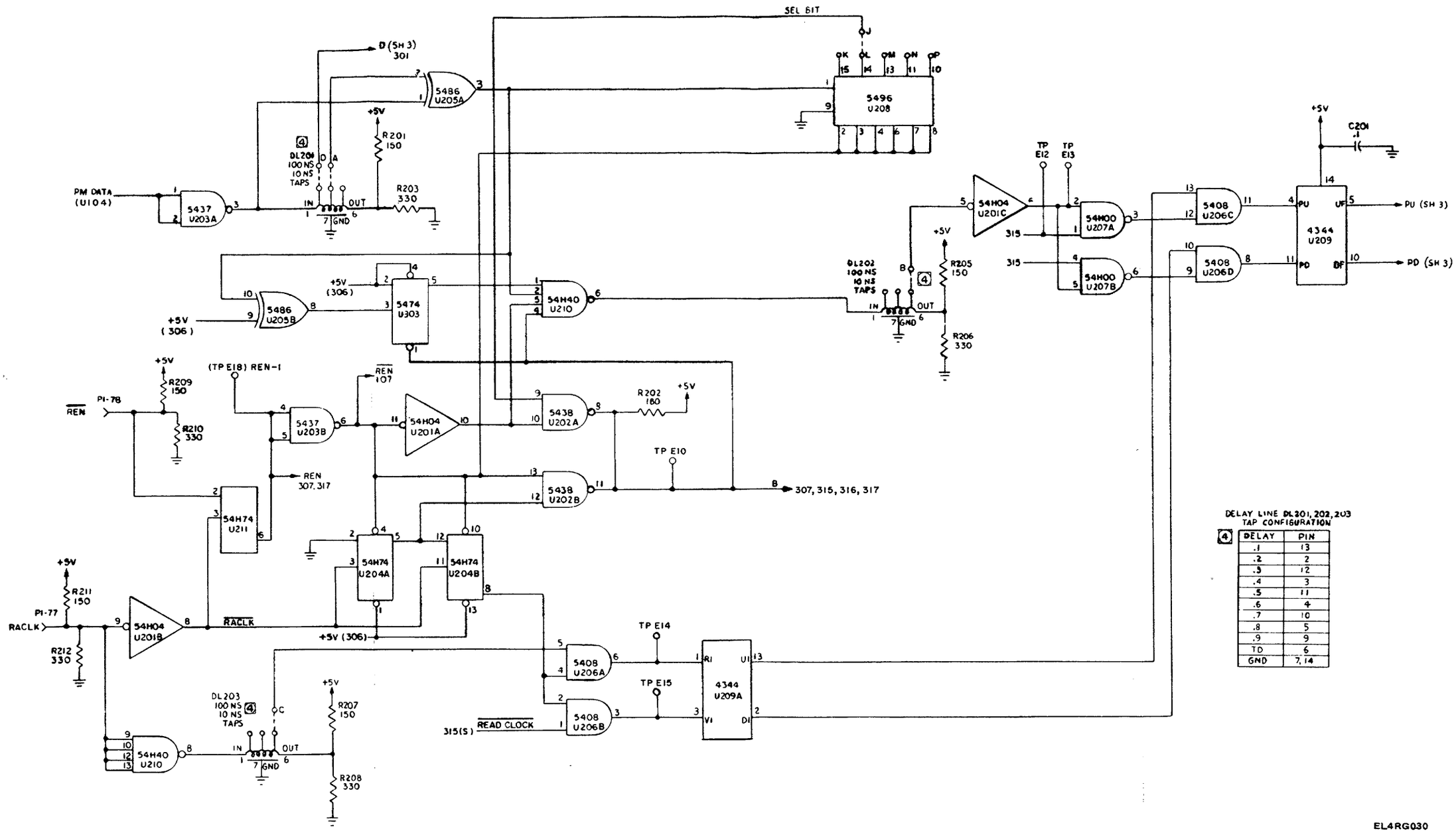
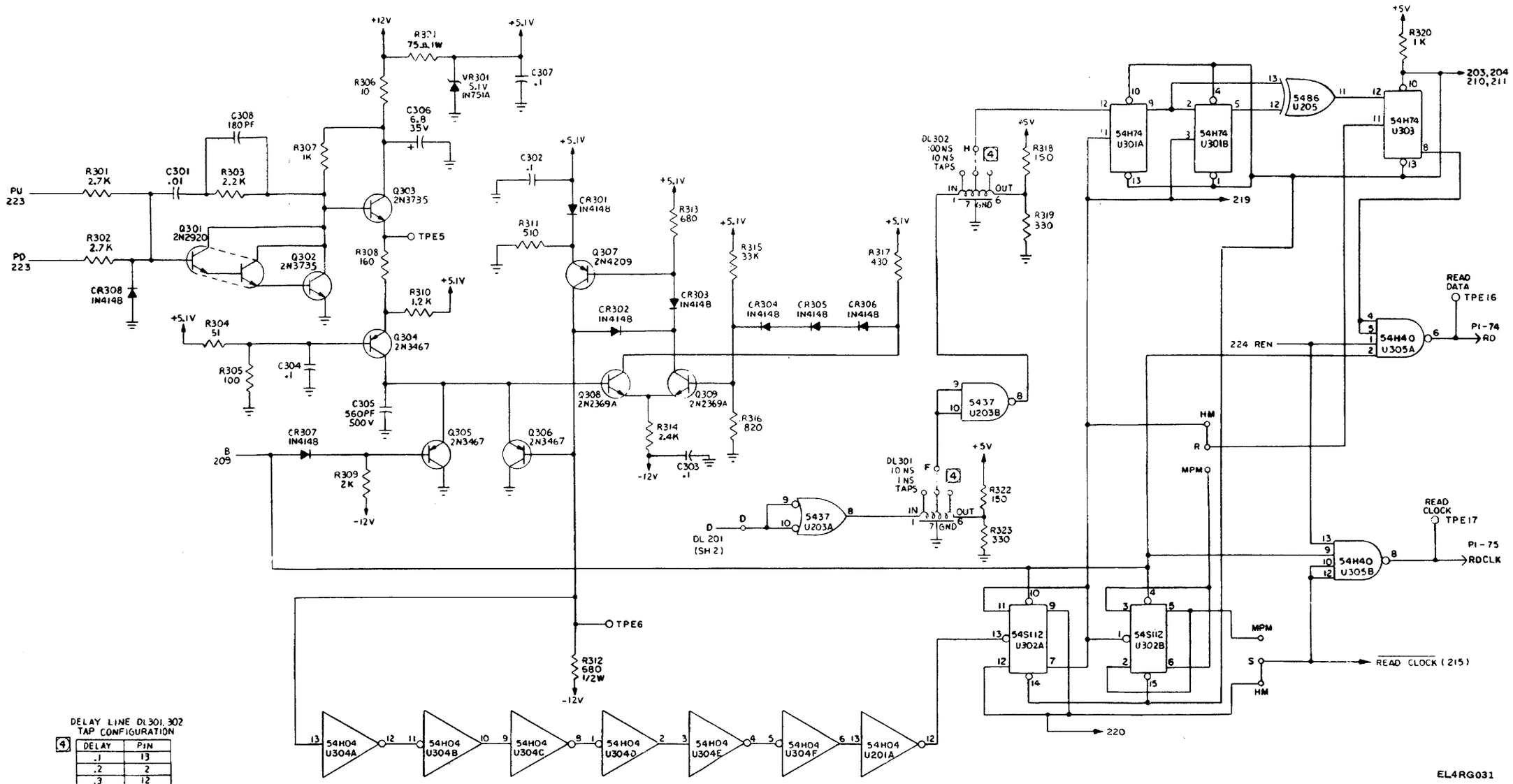


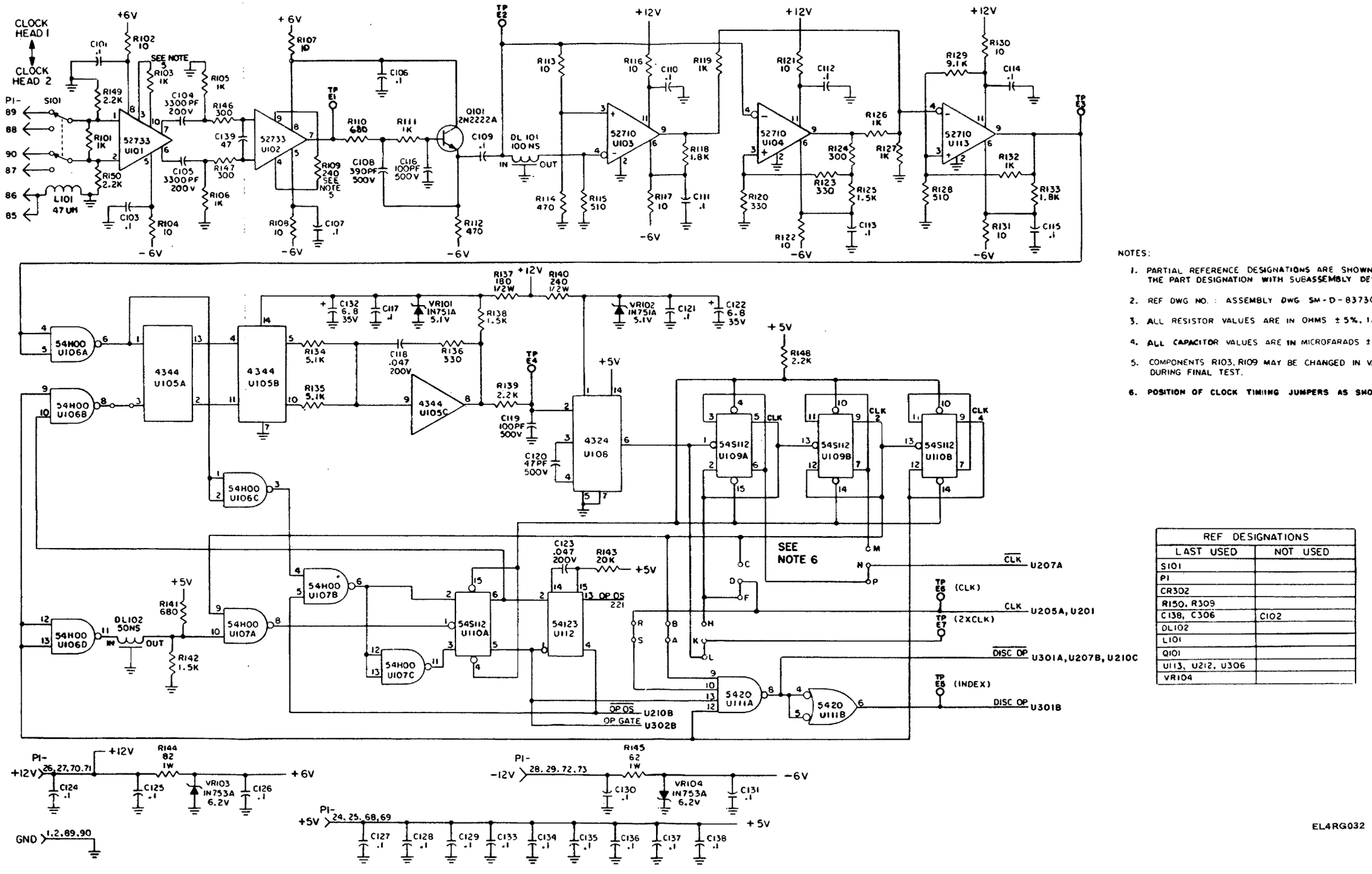
Figure FO-8. Data Read Amplifier Schematic Diagram (Sheet 2 of 3)



DELAY LINE DL301, 302
TAP CONFIGURATION

[4] DELAY	PIN
.1	13
.2	2
.3	12
.4	3
.5	11
.6	4
.7	10
.8	5
.9	9
TD	6

Figure FO-8. Data Read Amplifier Schematic Diagram (Sheet 3 of 3)

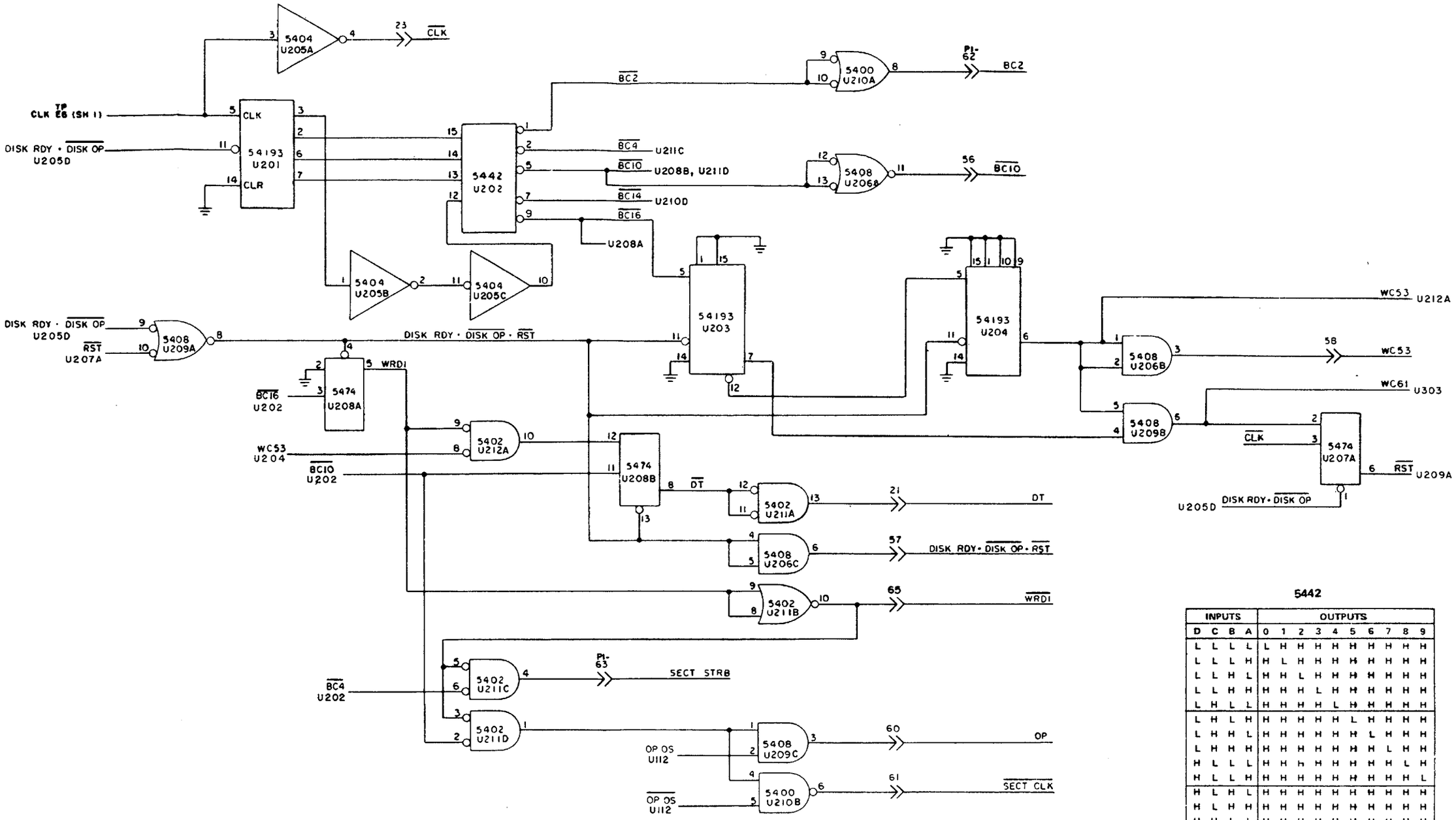


NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. PREFIX THE PART DESIGNATION WITH SUBASSEMBLY DESIGNATION.
2. REF DWG NO. : ASSEMBLY DWG SM-D-837308.
3. ALL RESISTOR VALUES ARE IN OHMS ±5%, 1/4 W
4. ALL CAPACITOR VALUES ARE IN MICROFARADS ±10%, 100V
5. COMPONENTS R103, R109 MAY BE CHANGED IN VALUE DURING FINAL TEST.
6. POSITION OF CLOCK TIMING JUMPERS AS SHOWN.

REF DESIGNATIONS	
LAST USED	NOT USED
S101	
P1	
CR302	
R150, R309	
C138, C306	C102
DL102	
L101	
Q101	
U113, U212, U306	
VR104	

Figure FO-9. Clock Amplifier Schematic Diagram (Sheet 1 of 3)



5442

INPUTS				OUTPUTS									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

EL4RG033

Figure FO-9. Clock Amplifier Schematic Diagram (Sheet 2 of 3)

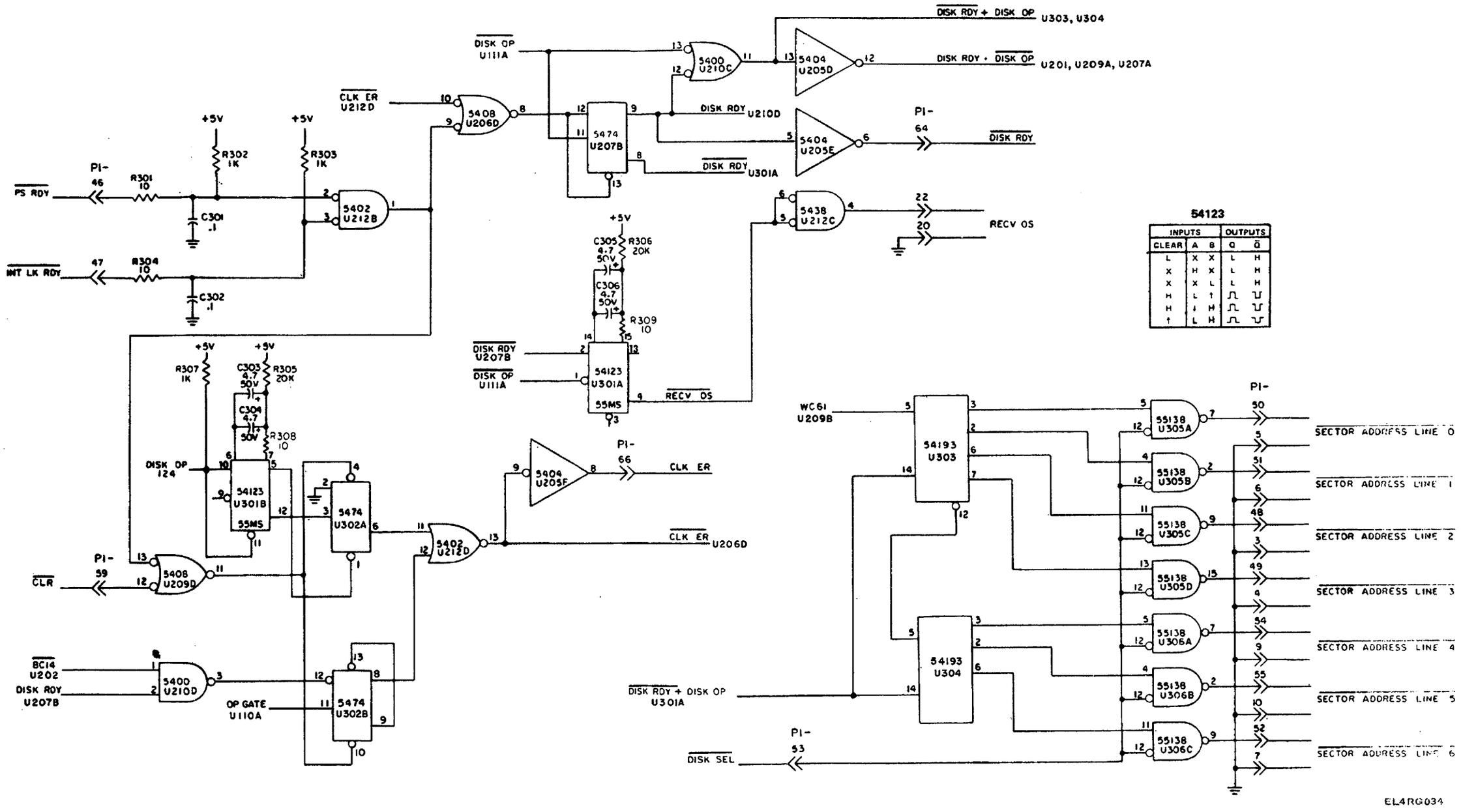
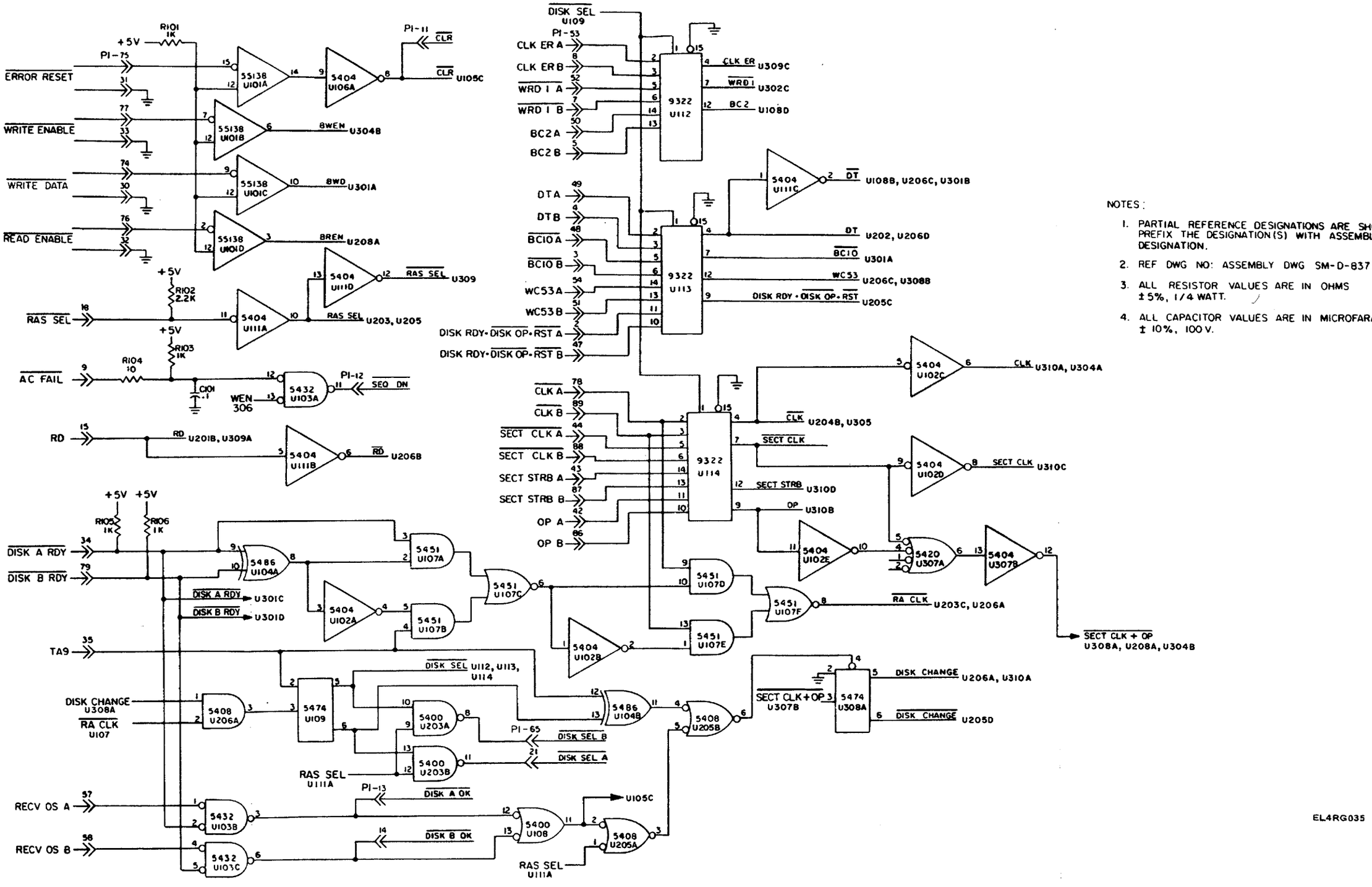


Figure FO-9. Clock Amplifier Schematic Diagram (Sheet 3 of 3)



NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. PREFIX THE DESIGNATION(S) WITH ASSEMBLY DESIGNATION.
2. REF DWG NO: ASSEMBLY DWG SM-D-837320.
3. ALL RESISTOR VALUES ARE IN OHMS ±5%, 1/4 WATT.
4. ALL CAPACITOR VALUES ARE IN MICROFARADS ±10%, 100 V.

Figure FO-10. Control Logic Diagram (Sheet 1 of 3)

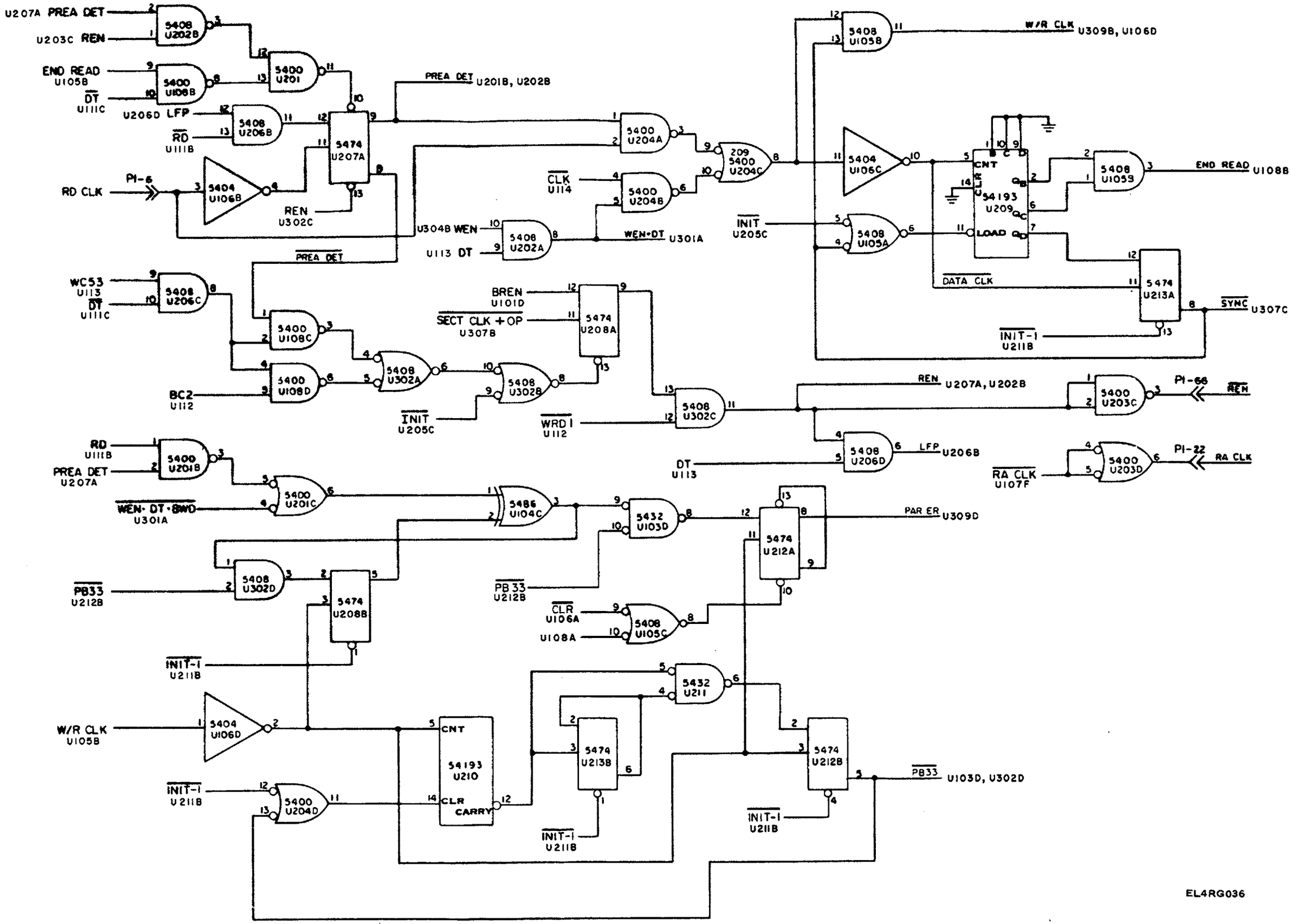
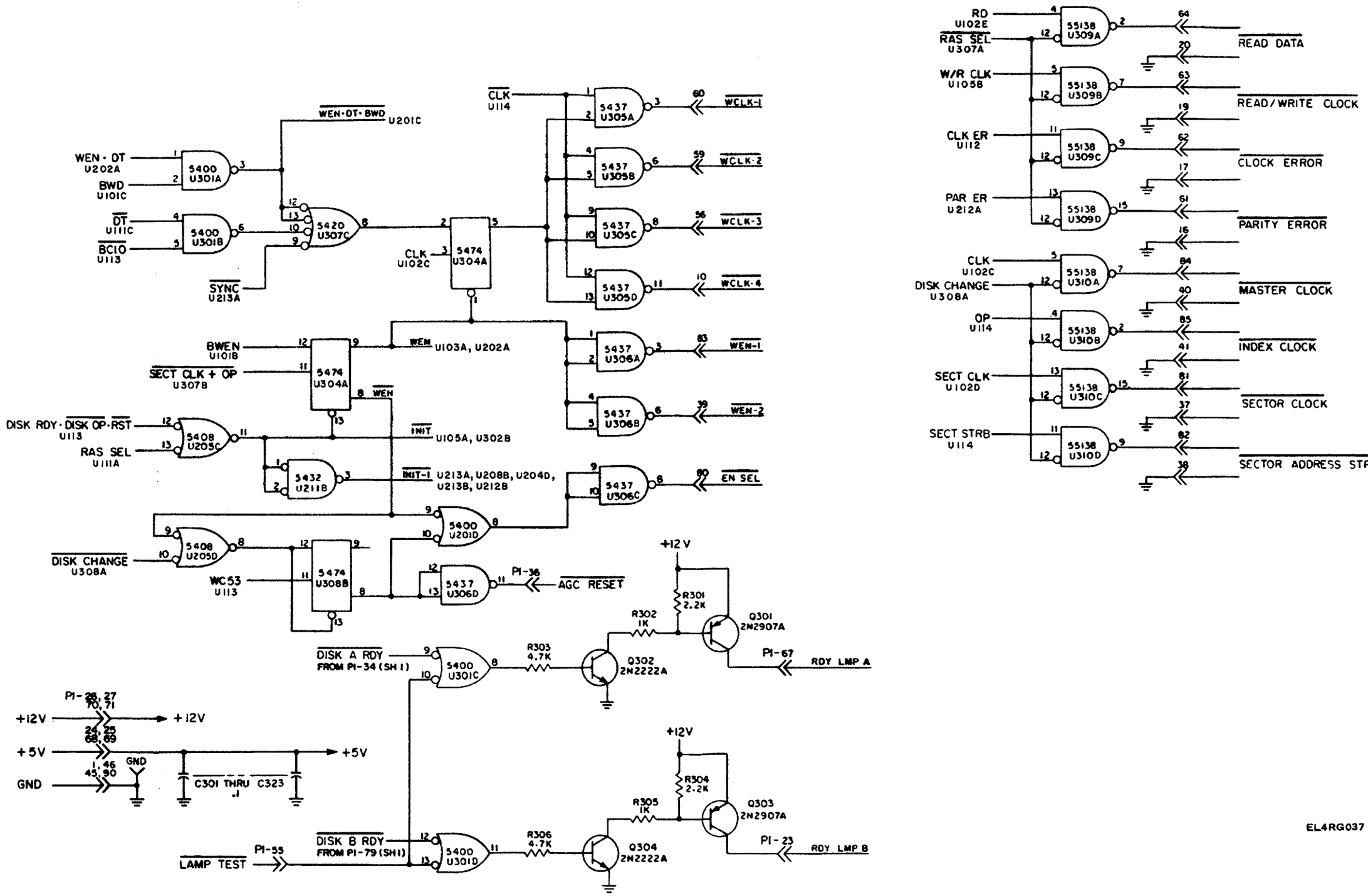
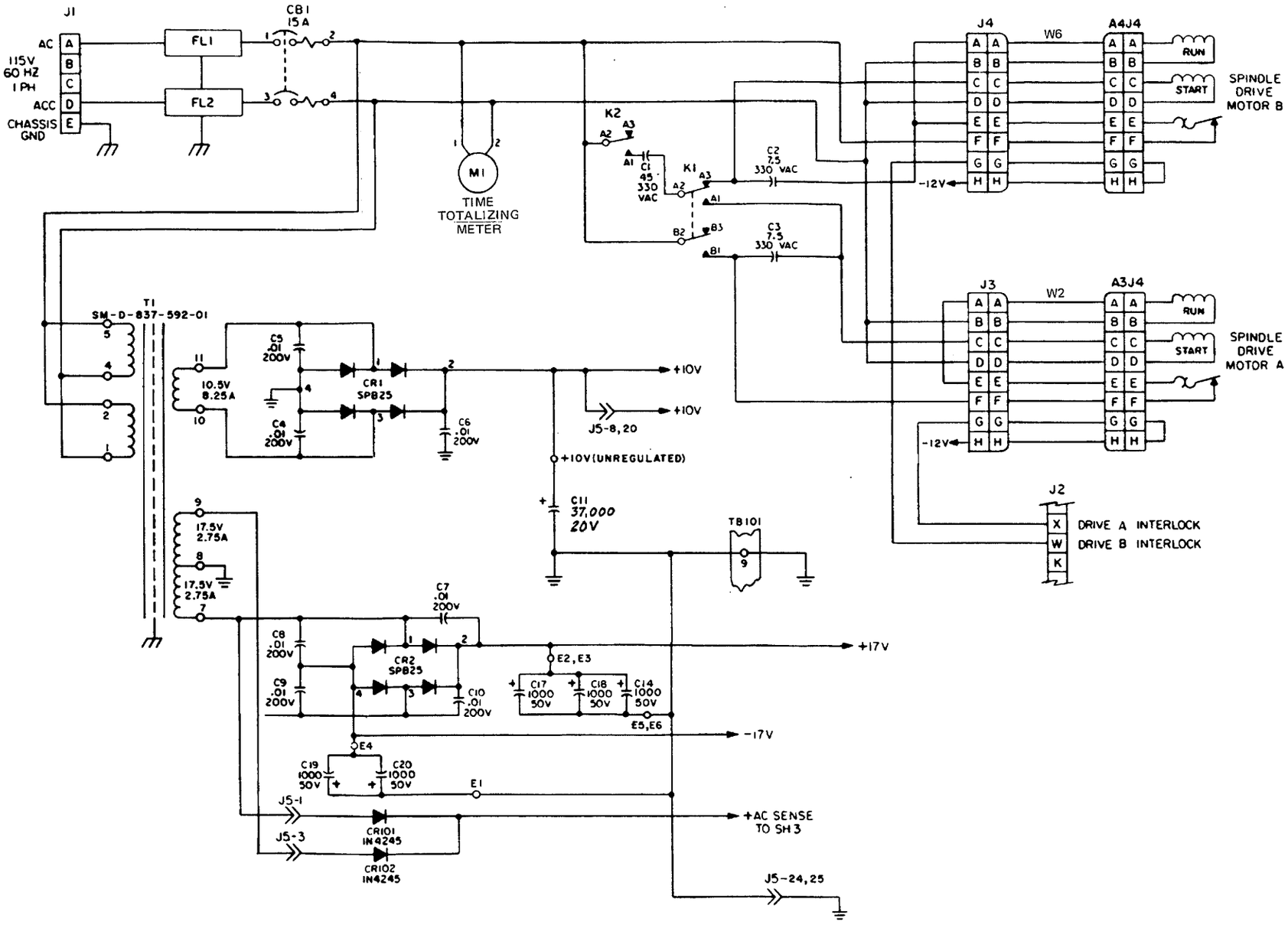


Figure FO-10. Control Logic Diagram (Sheet 2 of 3)



EL4RG037

Figure FO-10. Control Logic Diagram (Sheet 3 of 3)



NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. PREFIX THE PART DESIGNATIONS WITH SUBASSEMBLY DESIGNATION(S).
2. REF DWG NO: ASSEMBLY DWG SM-D-837588.
3. ALL RESISTOR VALUES ARE IN OHMS ± 5%, 1/4W.
4. ALL CAPACITOR VALUES ARE IN MICROFARADS ± 10%.
5. CONNECTOR J5 INTERCONNECTS CHASSIS WITH REGULATOR CIRCUIT CARD ASSEMBLY SM-D-837589.
6. COMPONENTS R202, R203, R213, R214, R223, R224, R304, R305, R318 SHALL BE SELECTED IN FINAL TEST.
7. COMPONENT R314 MAY BE SELECTED IN FINAL TEST.

EL4RG038

Figure FO-11. Power Supply Schematic Diagram (Sheet 1 of 5)

Change 1

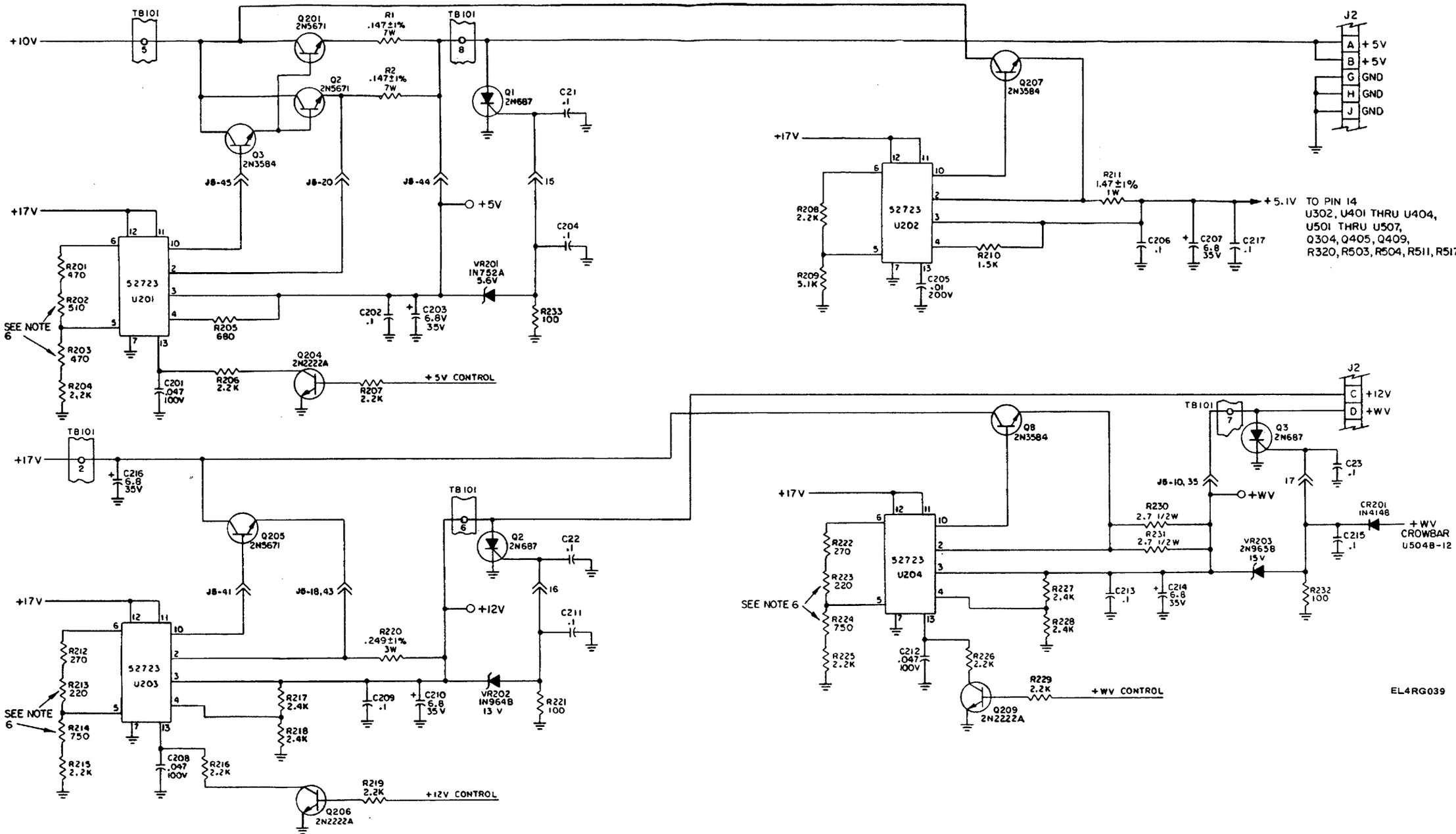


Figure FO-11. Power Supply Schematic Diagram (Sheet 2 of 5)

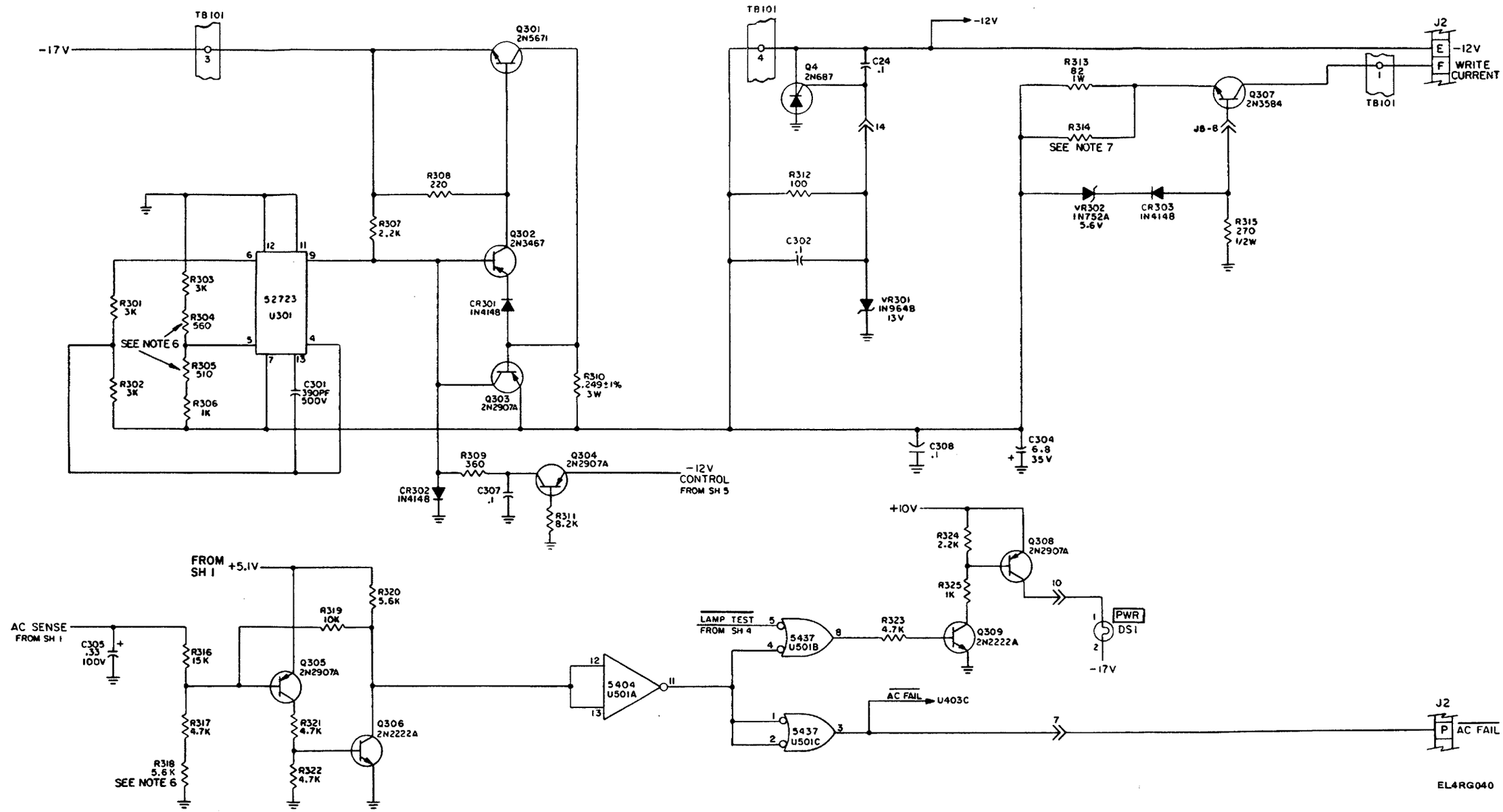


Figure FO-11. Power Supply Schematic Diagram (Sheet 3 of 5)

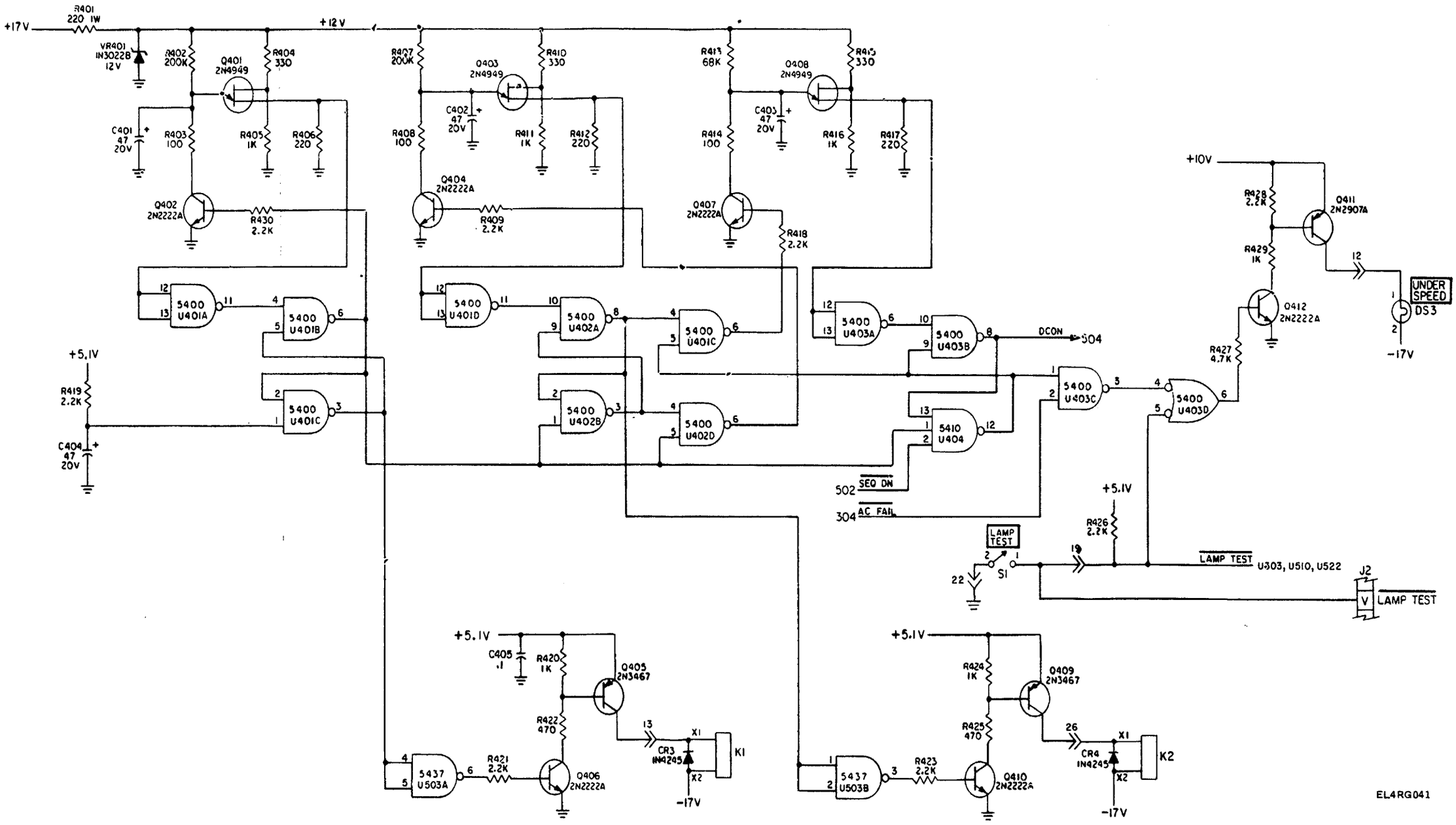


Figure FO-11. Power Supply Schematic Diagram (Sheet 4 of 5)

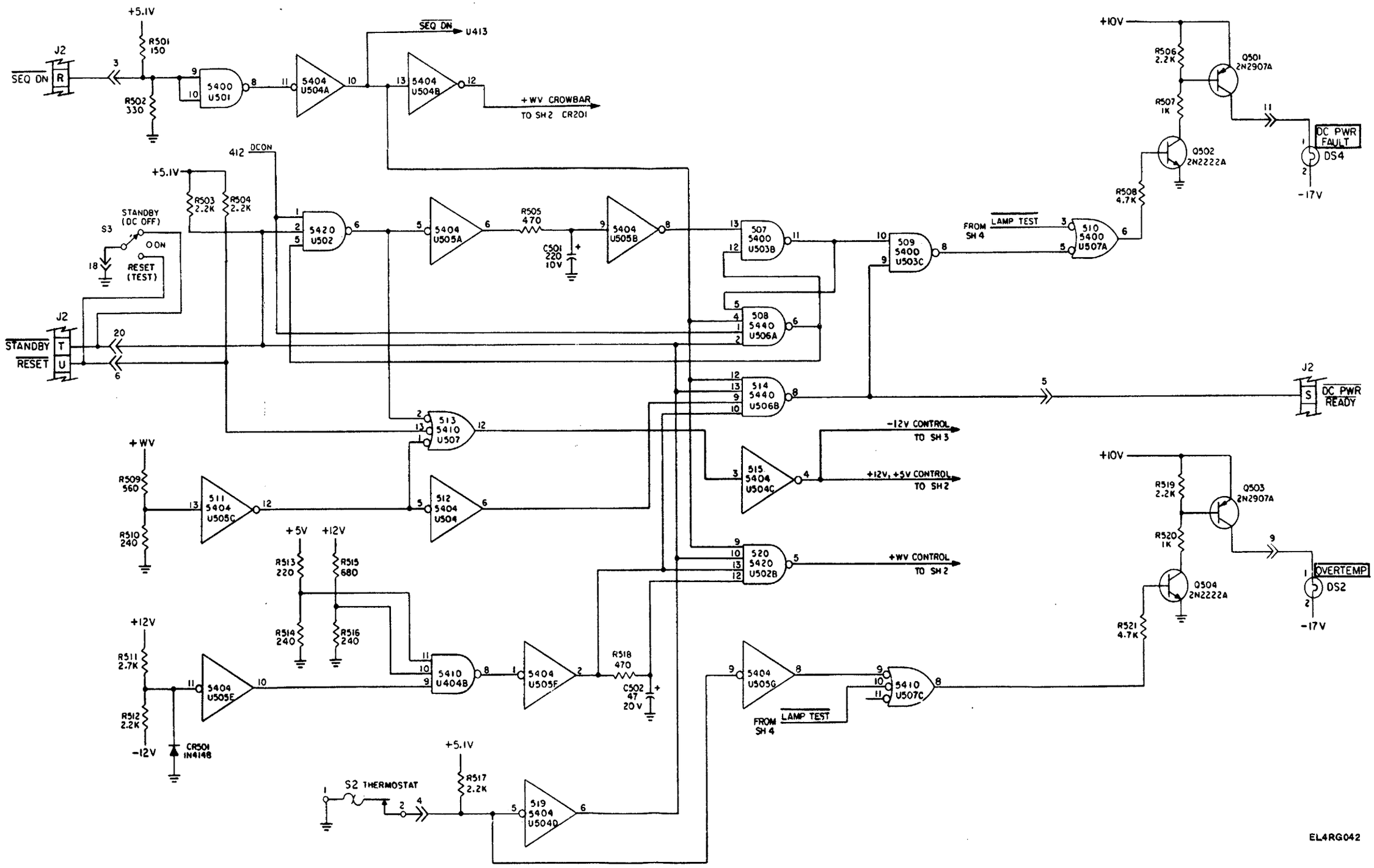
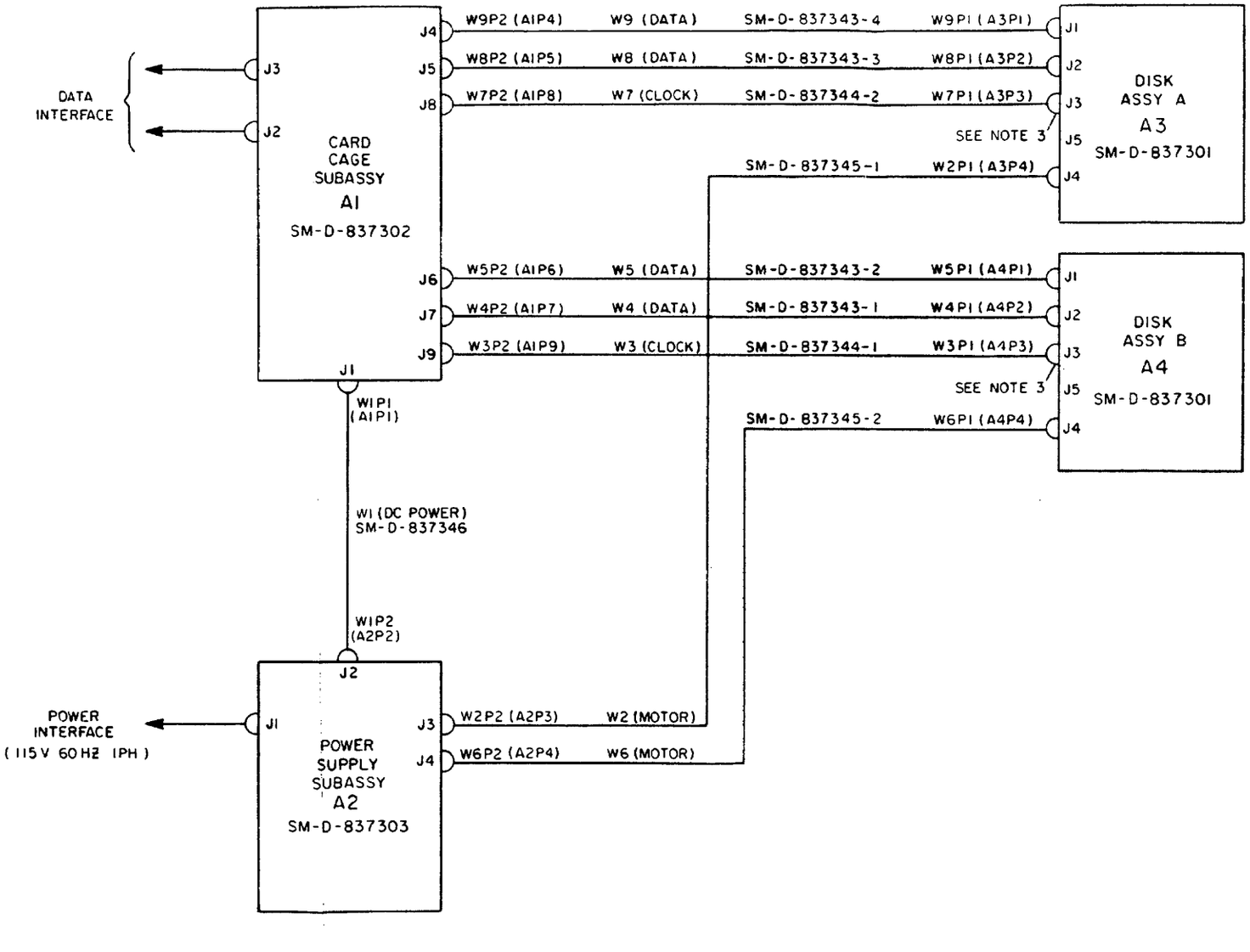


Figure FO-11. Power Supply Schematic Diagram (Sheet 5 of 5)

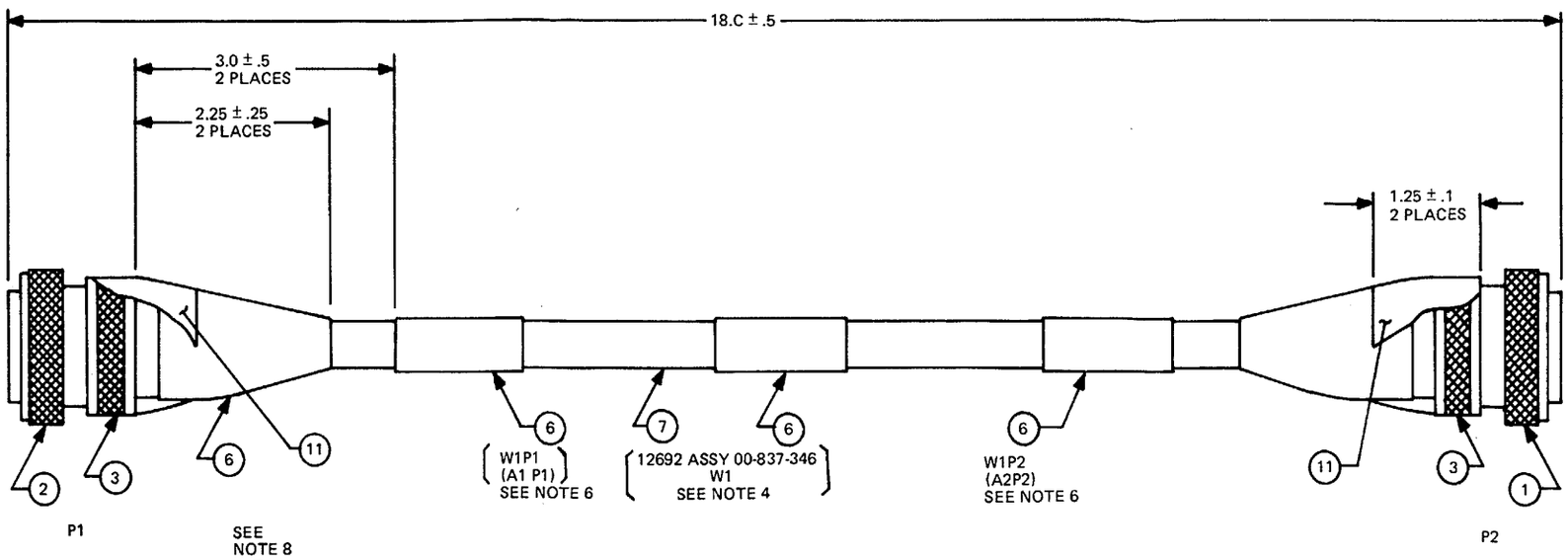


NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN PREFIX THE DESIGNATION(S) WITH ASSEMBLY . DESIGNATION.
2. REF DWG NO: ASSEMBLY DWG SM-D-837300.
3. SPARE CLOCK HEAD MAY BE SELECTED BY CONNECTING W7P1 AND W3P1 TO DISK CONNECTOR J5.

EL4RG043

Figure FO-12. Cable Interconnect Diagram



NOTES:

1. PART NO. IS 11160 ASSY 00-837-346-00.
2. TIE BRAID USING TWINE FIND NO. 10 EVERY 2 INCHES UNDER TUBING FIND NO. 7.
3. SHRINK INSULATION FIND NO. 6 & 11 BY APPLYING HEAT AT 200° ± 5°C UNIFORMLY AROUND INSULATION.
4. MARK FIND NO. 6 PER MIL-M-81531 WITH PART NO. AND APPLICABLE REV LTR AND CABLE REF DESIGNATION .12 CHARACTERS.
5. PINS SHALL BE CRIMPED USING TOOL M 22520/1-02 INSERT PINS WITH TOOL MS 3447-16.
6. MARK FIND NO. 6 PER MIL-M-81531 WITH APPLICABLE CONNECTOR IDENTIFICATION .12 CHARACTERS.
7. WIRE PER WIRE CHART.
8. ITEM 4 CRIMPED TO CAUSE BRAIDED SHIELD TO CONDUCT CHASSIS GROUND THROUGH CONNECTOR.

WIRE CHART

WIRE NO.	FIND NO.	FROM	TO	COLOR
1	8	PI-A	P2-A	WHITE
2	8	PI-B	P2-B	WHITE
3	8	PI-C	P2-C	WHITE
4	8	PI-D	P2-D	WHITE
5	8	PI-E	P2-E	WHITE
6	8	PI-F	P2-F	WHITE
7	9	PI-G	P2-G	BLACK
8	9	PI-H	P2-H	BLACK
9	9	PI-J	P2-J	BLACK
10	9	PI-K	P2-K	BLACK
11	8	PI-P	P2-P	WHITE
12	8	PI-R	P2-R	WHITE
13	8	PI-S	P2-S	WHITE
14	8	PI-T	P2-T	WHITE
15	8	PI-U	P2-U	WHITE
16	8	PI-V	P2-V	WHITE
17	8	PI-W	P2-W	WHITE
18	8	PI-X	P2-X	WHITE
SHLD	5	P1-SHELL	P2-SHELL	BRAID

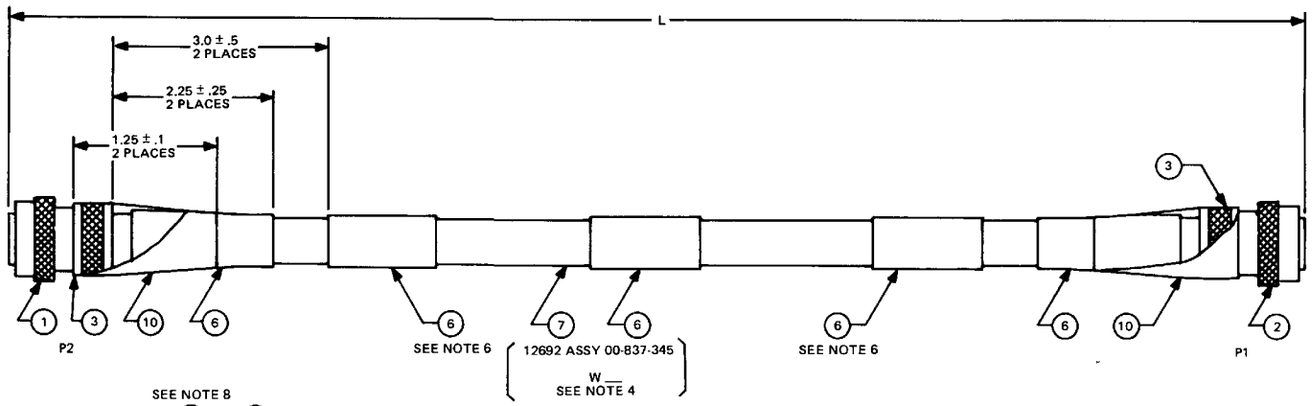
ITEM NO.	QUANTITY REQ'D		-00	SIZE	PART NO.	GAPL INDENTURE			DESCRIPTION	ASSY	GAPL PAGE NO.	CODE IDENT NO SPECIFICATIONS MATERIAL OR REMARKS
				D	00-837-346	X			CABLE ASSY			
1			1	A	17-160-402-00		X		CONNECTOR			MS3476E22-21P
2			1	A	17-160-409-00		X		CONNECTOR			MS3476E22-21S
3			2	A	17-183-098-02		X		BACKSHELL, SHIELD			MS3419-22N
4			2	A	17-681-041-02		X		RING, SHIELD CRIMP, PINK			MS5161-22
5			A/R	A	17-713-061-03		X		BRAID, WIRE, TUBULAR 5/8 INCH			QQ-B-575
6			A/R	A	17-713-059-02		X		INSULATION SLEEVING, BLK 5/8" HEAT-SHRINKABLE, BLK. 1 1/2"			MIL-23053/5 CLASS 1 BLACK
7			A/R	A	17-713-060-01		X		INSULATION SLEEVING, BLK 5/8"			MIL-I-7444 TYPE III CLASS 1 BLACK
8			A/R		17-957-270-09		X		WIRE, ELECTRICAL 16 AWG WHITE			MIL-W-16878/4 TYPE E-16
9			A/R		17-957-270-00		X		WIRE, ELECTRICAL 16 AWG BLACK			MIL-W-16878/4 TYPE E-16
10			A/R	A	17-175-009-00		X		TWINE, LACING			MIL-T-713 TYPE P, CLASS 1
11			A/R	A	17-713-059-04		X		INSULATION SLEEVING BLK. HEAT-SHRINKABLE 2"			MIL-I-23053/5 CLASS 1 BLACK

EL4RG046

Figure FO-13. Electrical Cable Assembly W1
Change 1

NOTES:

1. PART NO. IS 12692 ASSY 00-837-345-00 .
2. TIE BRAID USING TWINE FIND NO. 9 EVERY 2 INCHES UNDER TUBING FIND NO. 7 .
3. SHRINK INSULATION FIND NO. 6 & 10 BY APPLYING HEAT AT 200° ±5°C UNIFORMLY ARCUND INSULATION .
4. MARK FIND NO. 6 PER MIL-M-81531 WITH PART AND DASH NO. WITH APPLICABLE REV LTR & CABLE REF DESIGNATION .12 CHARACTERS .
5. PINS SHALL BE CRIMPED USING TOOL M 22520/0-02 INSERT PINS WITH TOOL MS 3447-16 .
6. MARK FIND NO. 6 PER MIL-M-81531 WITH APPLICABLE CONNECTOR IDENT. .12 HIGH CHARACTERS .
7. WIRE PER WIRE CHART.
8. ITEM 4 CRIMPED TO CAUSE BRAIDED SHIELD TO CONDUCT CHASSIS GROUND THROUGH CONNECTOR.



TABULATION BLOCK				
DASH NO	CABLE REF DES	LENGTH (L)	P1 IDENT	P2 IDENT
-01	W2	24.0 ± .5	W2 P1 A3 P4	W2 P2 A2 P3
-02	W6	18.0 ± .5	W6 P1 A4 P4	W6 P2 A2 P4

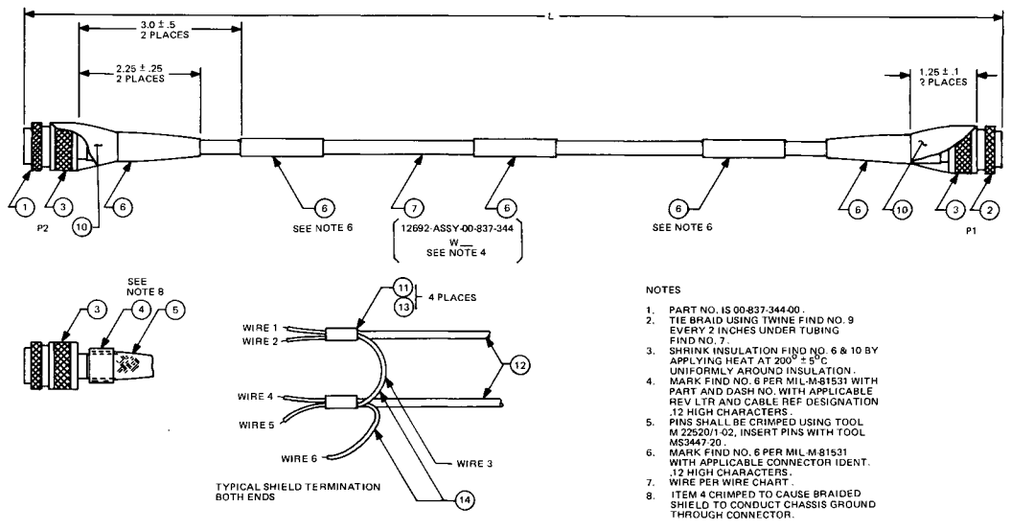
WIRE CHART				
WIRE NO.	FIND NO.	FROM	TO	COLOR
1	8	PI-A	P2-A	WHITE
2	8	PI-B	P2-B	WHITE
3	8	PI-C	P2-C	WHITE
4	8	PI-D	P2-D	WHITE
5	8	PI-E	P2-E	WHITE
6	8	PI-F	P2-F	WHITE
7	8	PI-G	P2-G	WHITE
8	8	PI-H	P2-H	WHITE
SHLD	5	P1-SHELL	P2-SHELL	BRAID

ITEM NO.	QUANTITY REQ'D -02	QUANTITY REQ'D -01	SIZE	PART NO.	GAPL INDENTURE			DESCRIPTION	ASSY	GAPL PAGE NO.	CODE IDENT NO SPECIFICATIONS MATERIAL OR REMARKS
			D	00-837-345		X		CABLE ASSY			
1	1	1	A	17-160-399-00			X	CONNECTOR			MS3476E16-8P
2	1	1	A	17-160-398-00			X	CONNECTOR			MS3476E16-8S
3	2	2	A	17-183-098-0			X	BACKSHELL, SHIELD, GRAY			MS3419-16N
4	2	2	A	17-681-041-01			X	RING, SHIELD, GRAY			MS3161-10
5	A/R	A/R	A	17-713-061-01			X	BRAID, WIRE, TUBULAR 3/8 INCH			QQ-B-575
6	A/R	A/R	A	17-713-059-01			X	INSULATION TUBING, ELECTRICAL HEAT-SHRINKABLE, BLK 1"			MIL-I-23053/5 CLASS I BLACK
7	A/R	A/R	A	17-713-060-01			X	INSULATION SLEEVING, BLACK 5/8"			MIL-I-7444 TYPE III CLASS BLACK
8	A/R	A/R	A	17-957-270-09			X	WIRE, ELECTRICAL 16 AWG WHITE			MIL-W-16878/4 TYPE E-16
9	A/R	A/R	A	17-175-009-00			X	TWINE, LACING			MIL-T-713 TYPE P, CLASS 1
10	A/R	A/R	A	17-813-059-02			X	INSULATION TUBING ELECTRICAL HEAT-SHRINKABLE BLK 1 1/2"			MIL-I-23053/5 CLASS I BLACK

EL4RG047

Figure FO-14. Electrical Cable Assemblies W2 and W6.

ITEM NO.	QUANTITY REQ'D			SIZE	PART NO.	GAPL INDENTURE			DESCRIPTION	ASSY	GAPL PAGE NO.	CODE IDENT NO SPECIFICATIONS MATERIAL OR REMARKS
		-02	-01									
				D	00-837-344	X			CABLE ASSY.			
1		1	1	A	17-160-408-00		X		CONNECTOR			MS3476E10-6S
2		1	1	A	17-160-397-00		X		CONNECTOR			MS3476E10-6P
3		2	2	A	17-183-098-00		X		BACKSHELL, SHIELD			MS3419-10N
4		2	2	A	17-681-041-00		X		RING, SHIELD			MS3161-10
5		A/R	A/R	A	17-713-061-00		X		BRAID, WIRE, TUBULAR 1/4 INCH			QQ-B-575
6		A/R	A/R	A	17-713-059-00		X		INSULATION TUBING, ELECTRICAL HEAT-SHRINKABLE, BLK 3/4 INCH			MIL-I-23053/5 CLASS I BLACK
7		A/R	A/R	A	17-713-060-00		X		INSULATION SLEEVING, BLK 1/2 INCH			MIL-I-7444 TYPE III CLASS BLACK
8												
9		A/R	A/R	A	17-175-009-00		X		TWINE, LACING			MIL-T-713 TYPE P, CLASS I
10		A/R	A/R	A	17-713-059-01		X		INSULATION, SLEEVING BLK HEAT-SHRINKABLE 1"			MIL-I-23053/5 CLASS I BLK
11		4	4	A	00-837-512-00		X		FERRULE, ELECT CABLE			
12		A/R	A/R	A	00-837-511-00		X		CABLE, 2 COND SHIELDED 30 AWG			
13		A/R	A/R	A	17-713-059-03		X		INSULATION TUBING ELECTRICAL			MIL-I-23053/5 CLASS I BLACK
14		A/R	A/R		17-952-110-0		X		WIRE, ELECTRICAL, 26 AWG BLK			MIL-W-16878 TYPE BN



NOTES

1. PART NO. IS 00-837-344-00.
2. TIE BRAID USING TWINE FIND NO. 9 EVERY 2 INCHES UNDER TUBING FIND NO. 7.
3. SHRINK INSULATION FIND NO. 6 & 10 BY APPLYING HEAT AT 200° ± 5°C UNIFORMLY AROUND INSULATION.
4. MARK FIND NO. 6 PER MIL-M-81531 WITH PART AND DASH NO. WITH APPLICABLE REV LTR AND CABLE REF DESIGNATION .12 HIGH CHARACTERS.
5. PINS SHALL BE CRIMPED USING TOOL M 22520/1-02, INSERT PINS WITH TOOL MS3447-20.
6. MARK FIND NO. 6 PER MIL-M-81531 WITH APPLICABLE CONNECTOR IDENT. .12 HIGH CHARACTERS.
7. WIRE PER WIRE CHART.
8. ITEM 4 CRIMPED TO CAUSE BRAIDED SHIELD TO CONDUCT CHASSIS GROUND THROUGH CONNECTOR.

TABULATION BLOCK				
DASH NO	CABLE REF DES	LENGTH L	P1 IDENT	P2 IDENT
-01	W3	18.0 ± .5	(W3 P1 A4 P3)	(W3 P2 A1 P9)
-02	W7	24.0 ± .5	(W7 P1 A3 P3)	(W7 P2 A1 P8)

WIRE CHART					
CABLE NO	WIRE NO	FIND NO	FROM	TO	COLOR
1	1	13	P1-A	P2-A	WHITE
	2	13	P1-C	P2-C	RED
	3	14	SHLD CA 1	SHLD CA 2	BLACK
2	4	13	P1-D	P2-D	WHITE
	5	13	P1-F	P2-F	RED
	6	14	P1-E	P2-E	BLACK
	7	14	P1-B	P2-B	BLACK
1 AND 2	SHLD	5	P1-SHELL	P2-SHELL	BRAID

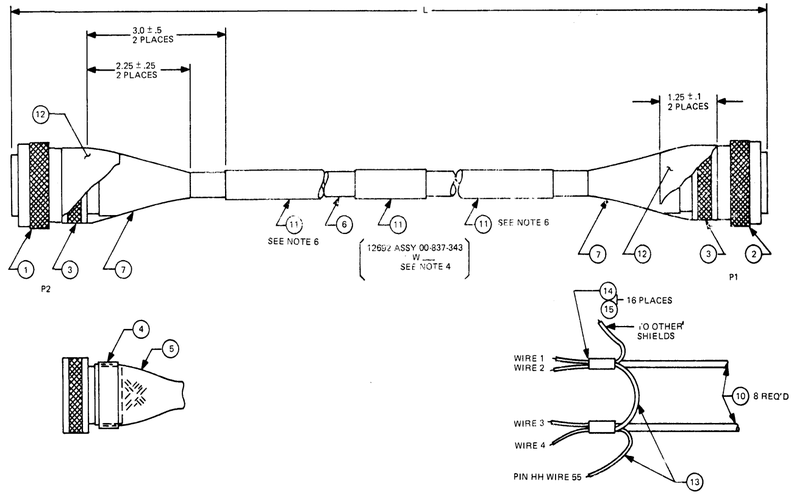
EL4RG048

Figure FO-15. Electrical Cable Assemblies W3 and W7.

QUANTITY REQ'D				ITEM NO.	SIZE	PART NO	INDENT		DESCRIPTION	ASSY	CODE IDENT NO SPECIFICATIONS MATERIAL OR REMARKS
-04	-03	-02	-01								
1	1	1	1	1	A	17-160-400-00	X		CONNECTOR		MS3476E22-55S
1	1	1	1	2	A	17-160-401-00	X		CONNECTOR		MS3476E22-55P
2	2	2	2	3	A	17-183-098-02	X		BACKSHELL, SHIELD		MS3419-22N
2	2	2	2	4	A	17-681-041-02	X		RING, SHIELD		MS3161-22
A/R	A/R	A/R	A/R	5	A	17-713-061-03	X		BRAID, WIRE TUBULAR 5/8"		QQ-B-575
A/R	A/R	A/R	A/R	6	A	17-713-060-01	X		INSULATION TUBING ELECTRICAL		MIL-I-7444 TYPE III
									5/8" BLACK		CLASS 1 BLK
A/R	A/R	A/R	A/R	7	A	17-713-059-02	X		INSULATION SLEEVING, 1 1/2", BLACK		MIL-23053/5
									HEAT-SHRINKABLE		CLASS 1 BLK
A/R	A/R	A/R	A/R	8	A	17-175-009-00	X		TWINE, LACING		MIL-T-713 TYPE P
											CLASS 1
A/R	A/R	A/R	A/R	9		17-952-110-00	X		WIRE, ELECTRICAL 26 AWG WHITE		MIL-W-16878 TYPE BN
A/R	A/R	A/R	A/R	10	A	00-837-511-00	X		CABLE, 30 AWG TWO COND, SHIELDED		
A/R	A/R	A/R	A/R	11	A	17-713-059-00	X		INSULATION SLEEVING' 3/4", BLK		MIL-I-23053/5
									HEAT-SHRINKABLE		CLASS 1 BLK
A/R	A/R	A/R	A/R	12	A	17-713-059-04	X		INSULATION SLEEVING 2" BLK		MIL-I-23053/5
									HEAT-SHRINKABLE		CLASS 1 BLK
A/R	A/R	A/R	A/R	13		17-952-110-00	X		WIRE ELECTRICAL 26 AWG BLK		MIL-W-16878
											TYPE DN
16	16	16	16	14	A	00-837-512-00	X		FERRULE ELECT. CABLE		
A/R	A/R	A/R	A/R	15	A	17-713-059-03	X		INSULATION TUBING ELECTRICAL		MIL-I-23053/5
											CLASS I BLK

WIRE CHART					
CABLE NO	WIRE NO	FIND NO	FROM	TO	COLOR
1	1	10	P1-A	P2-A	WHITE
	2	10	P1-V	P2-V	RED
2	3	10	P1-B	P2-B	WHITE
	4	10	P1-W	P2-W	RED
3	5	10	P1-C	P2-C	WHITE
	6	10	P1-X	P2-X	RED
4	7	10	P1-D	P2-D	WHITE
	8	10	P1-Y	P2-Y	RED
5	9	10	P1-E	P2-E	WHITE
	10	10	P1-Z	P2-Z	RED
6	11	10	P1-F	P2-F	WHITE
	12	10	P1-a	P2-a	RED
7	13	10	P1-G	P2-G	WHITE
	14	10	P1-b	P2-b	RED
8	15	10	P1-H	P2-H	WHITE
	16	10	P1-c	P2-c	RED
	17	9	P1-J	P2-J	WHITE
	18	9	P1-K	P2-K	WHITE
	19	9	P1-L	P2-L	WHITE
	20	9	P1-M	P2-M	WHITE
	21	9	P1-N	P2-N	WHITE
	22	9	P1-P	P2-P	WHITE
	23	9	P1-R	P2-R	WHITE
	24	9	P1-S	P2-S	WHITE
	25	9	P1-T	P2-T	WHITE
	26	9	P1-U	P2-U	WHITE
	27	9	P1-d	P2-d	WHITE
	28	9	P1-e	P2-e	WHITE

WIRE CHART				
WIRE NO	FIND NO	FROM	TO	COLOR
29	9	P1-f	P2-f	WHITE
30	9	P1-g	P2-g	WHITE
31	9	P1-h	P2-h	WHITE
32	9	P1-i	P2-i	WHITE
33	9	P1-j	P2-j	WHITE
34	9	P1-k	P2-k	WHITE
35	9	P1-m	P2-m	WHITE
36	9	P1-n	P2-n	WHITE
37	9	P1-p	P2-p	WHITE
38	9	P1-q	P2-q	WHITE
39	9	P1-r	P2-r	WHITE
40	9	P1-s	P2-s	WHITE
41	9	P1-t	P2-t	WHITE
42	9	P1-u	P2-u	WHITE
43	9	P1-v	P2-v	WHITE
44	9	P1-w	P2-w	WHITE
45	9	P1-x	P2-x	WHITE
46	9	P1-y	P2-y	WHITE
47	9	P1-z	P2-z	WHITE
48	9	P1-AA	P2-AA	WHITE
49	9	P1-BB	P2-BB	WHITE
50	9	P1-CC	P2-CC	WHITE
51	9	P1-DD	P2-DD	WHITE
52	9	P1-EE	P2-EE	WHITE
53	9	P1-FF	P2-FF	WHITE
54	9	P1-GG	P2-GG	WHITE
55	13	P1-HH	P2-HH	BLACK



TABULATION BLOCKK				
DASH NO	CABLE REF DES	LENGTH (L)	P1 IDENT	P2 IDENT
-01	W4	24.0 ± .5	W4 P1, A4 P2	W4 P2, A1 P7
-02	W5	24.0 ± .5	W5 P1, A4 P1	W5 P2, A1 P6
-03	W8	30.0 ± .5	W8 P1, A3 P2	W8 P2, A1 P5
-04	W9	30.0 ± .5	W9 P1, A3 P1	W9 P2, A1 P4

NOTES:

1. PART NO. IS 12692 ASSY 00-837-343-00.
2. TIE BRAID USING TWINE FIND NO. 8 EVERY 2 INCHES UNDER TUBING FIND NO. 7.
3. SHRINK INSULATION FIND NO. 7, 11, 12, BY APPLYING HEAT AT 200° ± 5°C UNIFORMLY AROUND INSULATION.
4. MARK FIND NO. 11 PER MIL-M-81531 WITH PART AND DASH NO. WITH APPLICABLE REV LTR AND CABLE REF DES .12 HIGH CHARACTERS.
5. PINS SHALL BE CRIMPED USING TOOL M 22520/1-02, INSERT PINS WITH TOOL MS 3447-20.
6. MARK FIND NO. 11 PER MIL-M-81531 WITH APPLICABLE CONNECTOR IDENTIFICATION .12 HIGH CHARACTERS.
7. WIRE PER WIRE CHART.

EL4RG049

Figure FO-16. Electrical Cable Assemblies W4, W5, W8 and W9.

RECOMMENDED CHANGES TO EQUIPMENT TECHNICAL PUBLICATIONS

THEN...JOT DOWN THE DOPE ABOUT IT ON THIS FORM. CAREFULLY TEAR IT OUT, FOLD IT AND DROP IT IN THE MAIL.

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FROM: (PRINT YOUR UNIT'S COMPLETE ADDRESS)

DATE SENT

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BE EXACT PIN-POINT WHERE IT IS

PAGE NO.	PARA-GRAPH	FIGURE NO.	TABLE NO.

IN THIS SPACE, TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT.

PRINTED NAME, GRADE OR TITLE AND TELEPHONE NUMBER	SIGN HERE

DA FORM 1 JUL 79 2028-2

PREVIOUS EDITIONS ARE OBSOLETE.

P.S.--IF YOUR OUTFIT WANTS TO KNOW ABOUT YOUR RECOMMENDATION MAKE A CARBON COPY OF THIS AND GIVE IT TO YOUR HEADQUARTERS.

The Metric System and Equivalents

Linear Measure

1 centimeter = 10 millimeters = .39 inch
1 decimeter = 10 centimeters = 3.94 inches
1 meter = 10 decimeters = 39.37 inches
1 dekameter = 10 meters = 32.8 feet
1 hectometer = 10 dekameters = 328.08 feet
1 kilometer = 10 hectometers = 3,280.8 feet

Weights

1 centigram = 10 milligrams = .15 grain
1 decigram = 10 centigrams = 1.54 grains
1 gram = 10 decigram = .035 ounce
1 decagram = 10 grams = .35 ounce
1 hectogram = 10 decagrams = 3.52 ounces
1 kilogram = 10 hectograms = 2.2 pounds
1 quintal = 100 kilograms = 220.46 pounds
1 metric ton = 10 quintals = 1.1 short tons

Liquid Measure

1 centiliter = 10 milliters = .34 fl. ounce
1 deciliter = 10 centiliters = 3.38 fl. ounces
1 liter = 10 deciliters = 33.81 fl. ounces
1 dekaliter = 10 liters = 2.64 gallons
1 hectoliter = 10 dekaliters = 26.42 gallons
1 kiloliter = 10 hectoliters = 264.18 gallons

Square Measure

1 sq. centimeter = 100 sq. millimeters = .155 sq. inch
1 sq. decimeter = 100 sq. centimeters = 15.5 sq. inches
1 sq. meter (centare) = 100 sq. decimeters = 10.76 sq. feet
1 sq. dekameter (are) = 100 sq. meters = 1,076.4 sq. feet
1 sq. hectometer (hectare) = 100 sq. dekameters = 2.47 acres
1 sq. kilometer = 100 sq. hectometers = .386 sq. mile

Cubic Measure

1 cu. centimeter = 1000 cu. millimeters = .06 cu. inch
1 cu. decimeter = 1000 cu. centimeters = 61.02 cu. inches
1 cu. meter = 1000 cu. decimeters = 35.31 cu. feet

Approximate Conversion Factors

To change	*To*	*Multiply by*	*To change*	*To*	*Multiply by*
inches	centimeters	2.540	ounce-inches	Newton-meters	.007062
feet	meters	.305	centimeters	inches	.394
yards	meters	.914	meters	feet	3.280
miles	kilometers	1.609	meters	yards	1.094
square inches	square centimeters	6.451	kilometers	miles	.621
square feet	square meters	.093	square centimeters	square inches	.155
square yards	square meters	.836	square meters	square feet	10.764
square miles	square kilometers	2.590	square meters	square yards	1.196
acres	square hectometers	.405	square kilometers	square miles	.386
cubic feet	cubic meters	.028	square hectometers	acres	2.471
cubic yards	cubic meters	.765	cubic meters	cubic feet	35.315
fluid ounces	milliliters	29,573	cubic meters	cubic yards	1.308
pints	liters	.473	milliliters	fluid ounces	.034
quarts	liters	.946	liters	pints	2.113
gallons	liters	3.785	liters	quarts	1.057
ounces	grams	28.349	liters	gallons	.264
pounds	kilograms	.454	grams	ounces	.035
short tons	metric tons	.907	kilograms	pounds	2.205
pound-feet	Newton-meters	1.356	metric tons	short tons	1.102
pound-inches	Newton-meters	.11296			

Temperature (Exact)

°F	Fahrenheit temperature	5/9 (after subtracting 32)	Celsius temperature	°C

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